

# Minilake M/B

PCB REV: C  
PCBA REV: C3A  
FAB: 3  
SCH Rev: 1.0  
LAST UPDATE: 2018/09/20

COVER PAGE

|                                                                                            |            |                                |           |                       |               |
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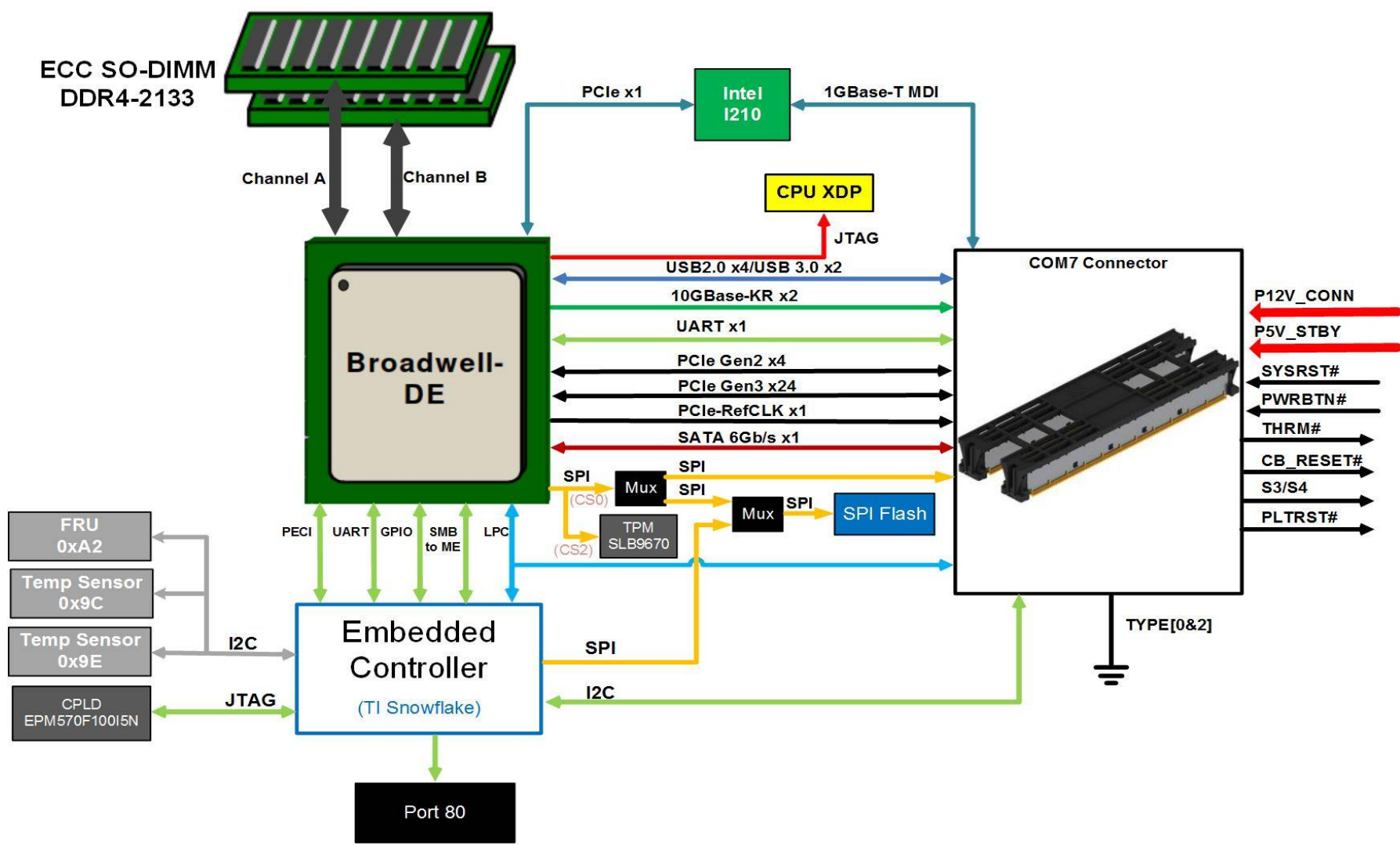
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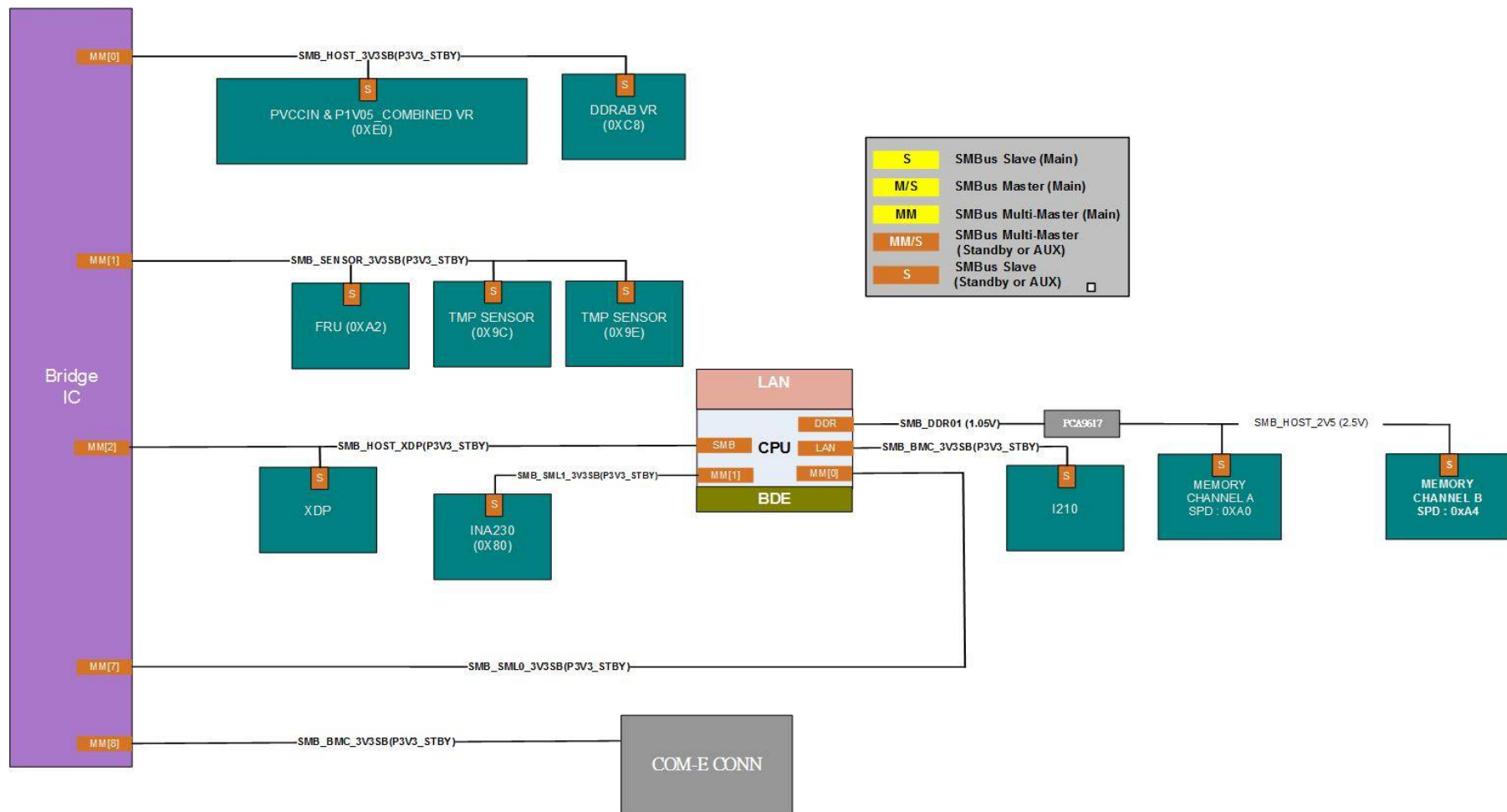
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[illegible]



Mini Lake BLOCK DIAGRAM



## SMBUS BLOCK DIAGRAM

**Quanta**

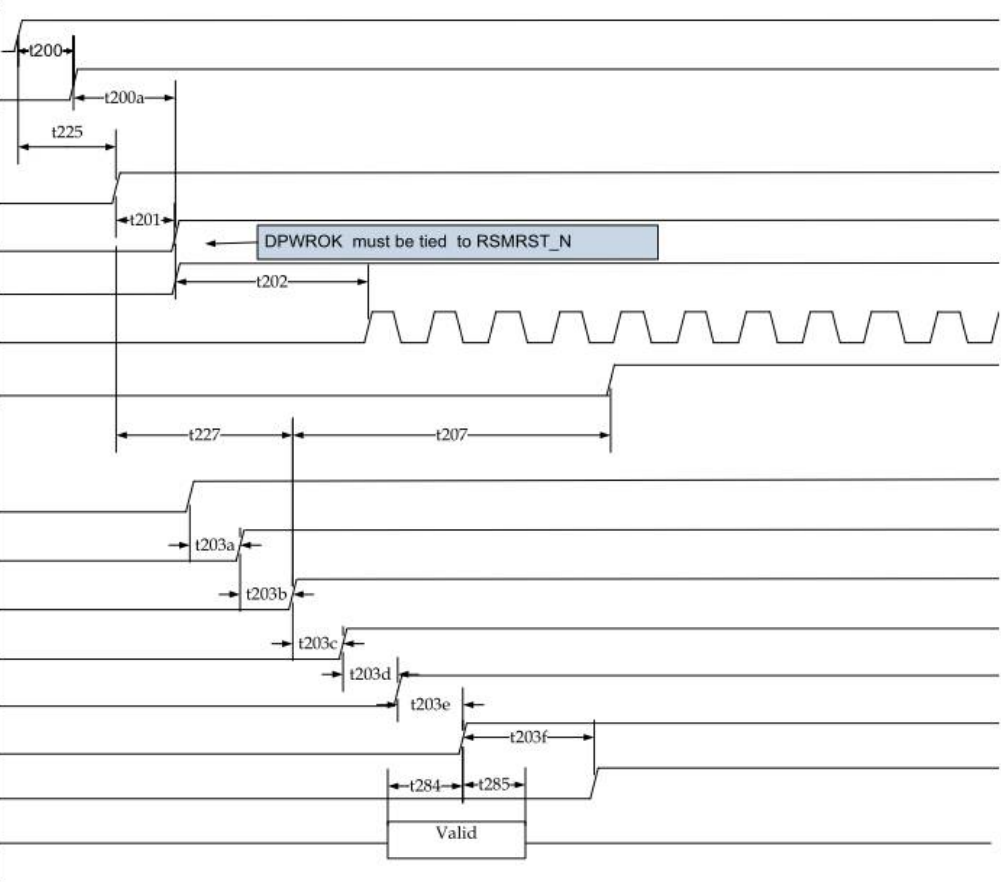
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| Source | Dest | Signal Name |
|--------|------|-------------|
|--------|------|-------------|

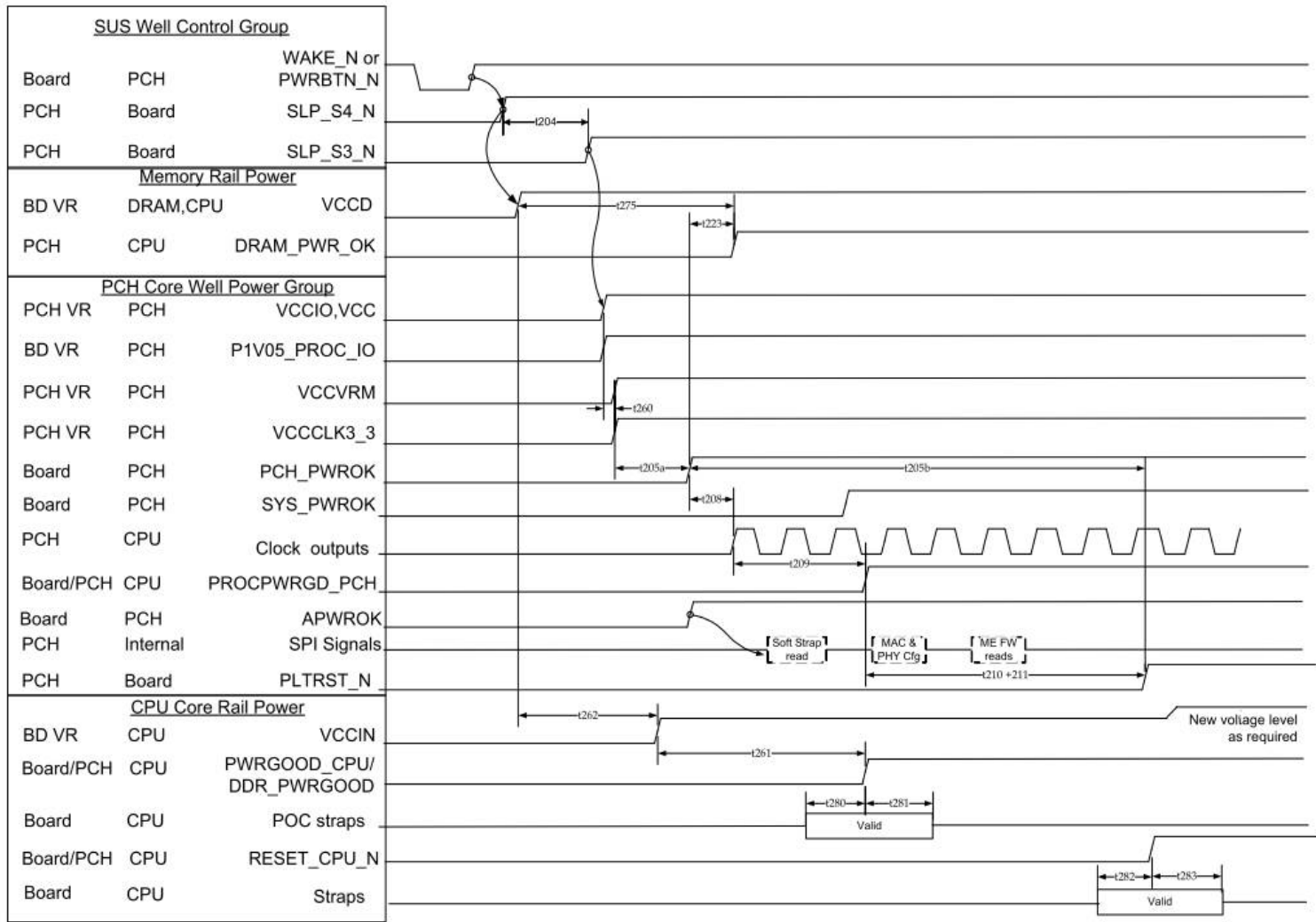
|                             |     |          |
|-----------------------------|-----|----------|
| <u>RTC Well Power Group</u> |     |          |
| Board                       | PCH | VCCRTC   |
| Board                       | PCH | RTCRST_N |

|                             |       |           |
|-----------------------------|-------|-----------|
| <u>SUS Well Power Group</u> |       |           |
| BD VR                       | PCH   | VCCSUS3_3 |
| Board                       | PCH   | DPWROK    |
| Board                       | PCH   | RSMRST_N  |
| PCH                         | Board | SUSCLK    |
| Board                       | PCH   | APWROK    |

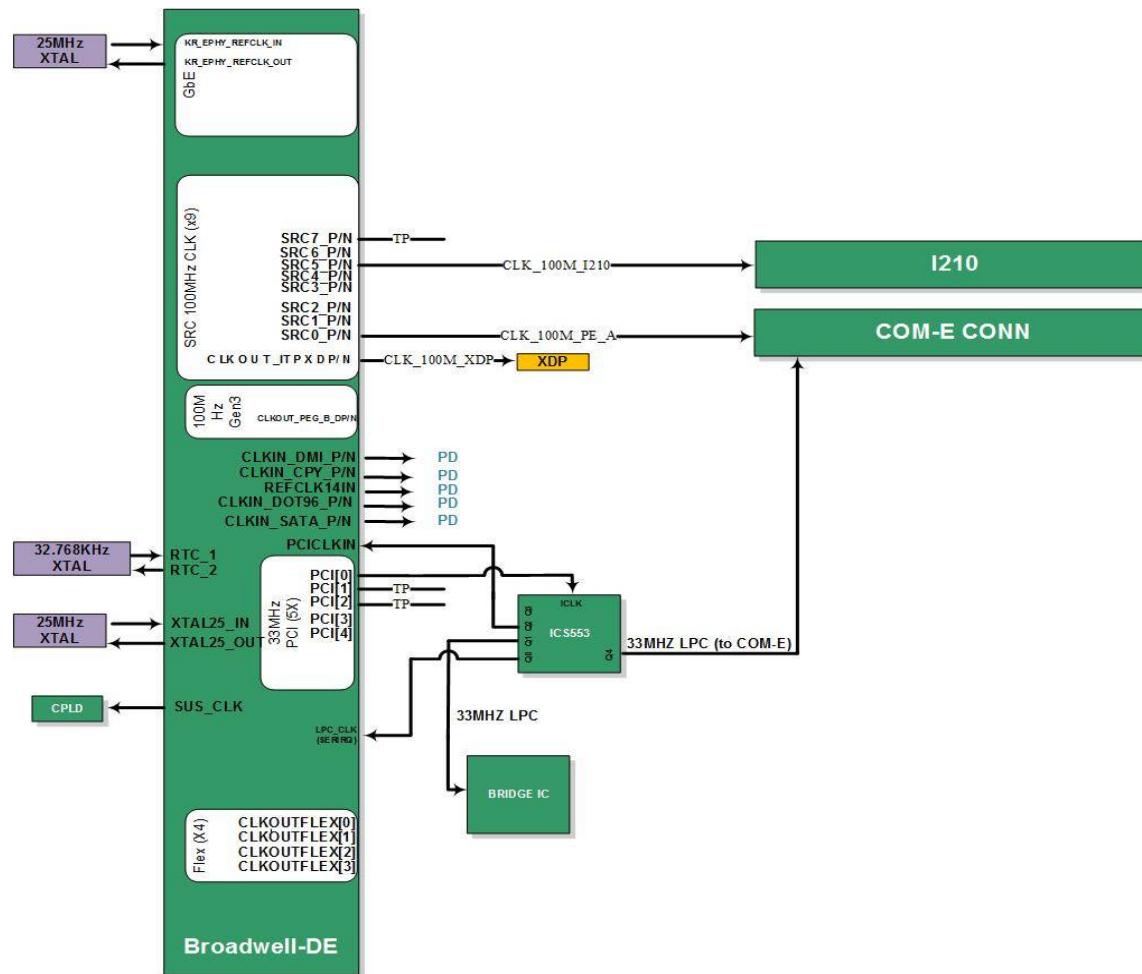
|                                  |     |              |
|----------------------------------|-----|--------------|
| <u>South Complex Power Group</u> |     |              |
| BD VR                            | CPU | VCCSCFUSESUS |
| BD VR                            | CPU | VCCKRHV      |
| BD VR                            | CPU | VCCIOIN      |
| BD VR                            | CPU | VCCGBE       |
| BD VR                            | CPU | VCCSCSUS     |
| Board                            | CPU | LAN_PWRGOOD  |
| Board                            | CPU | RSMRST_CPU_N |
| Board                            | CPU | Straps       |



POWER SEQUENCE DIAGRAM 1



POWER SEQUENCE DIAGRAM\_2

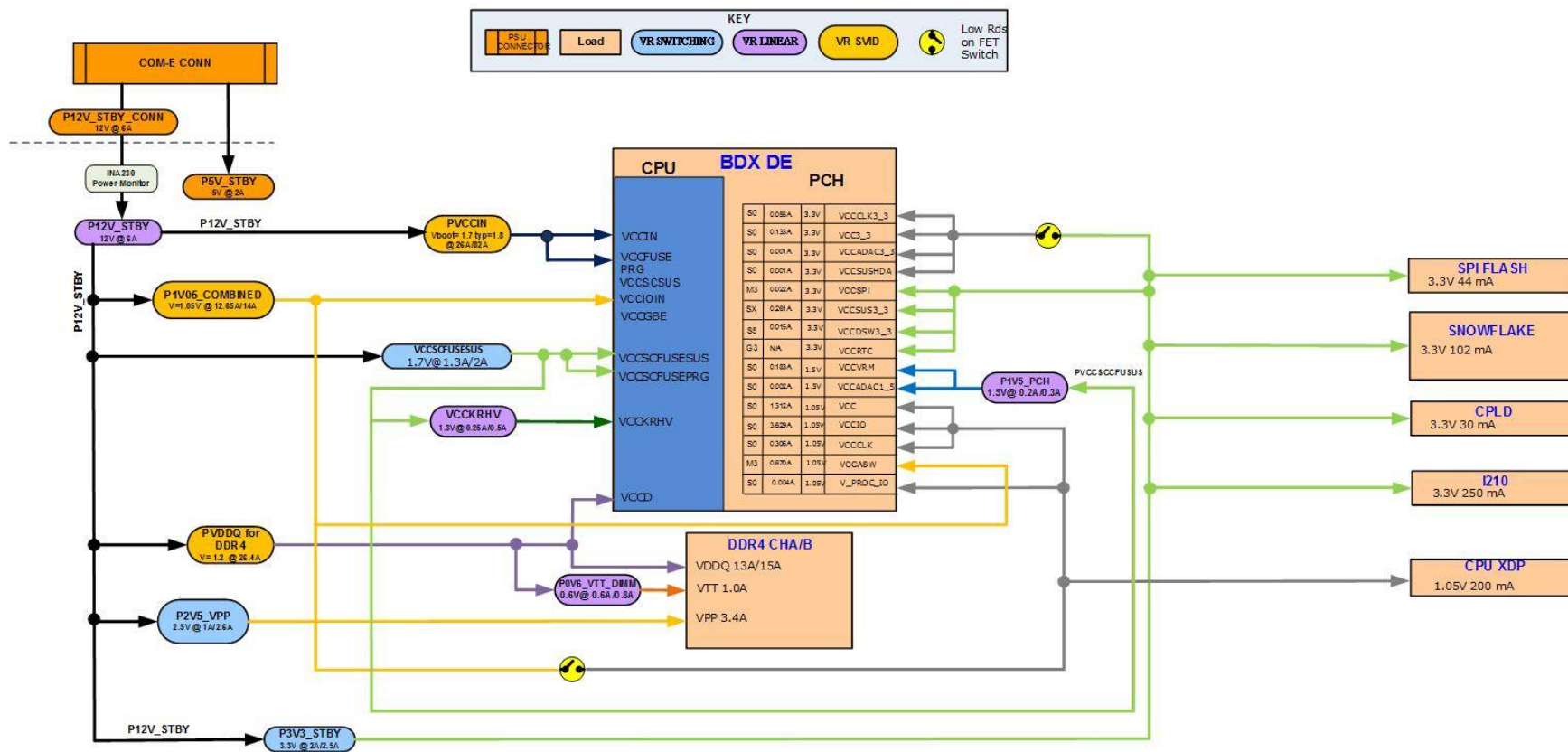


CLOCK DIAGRAM





# Mini Lake POWER DIAGRAM

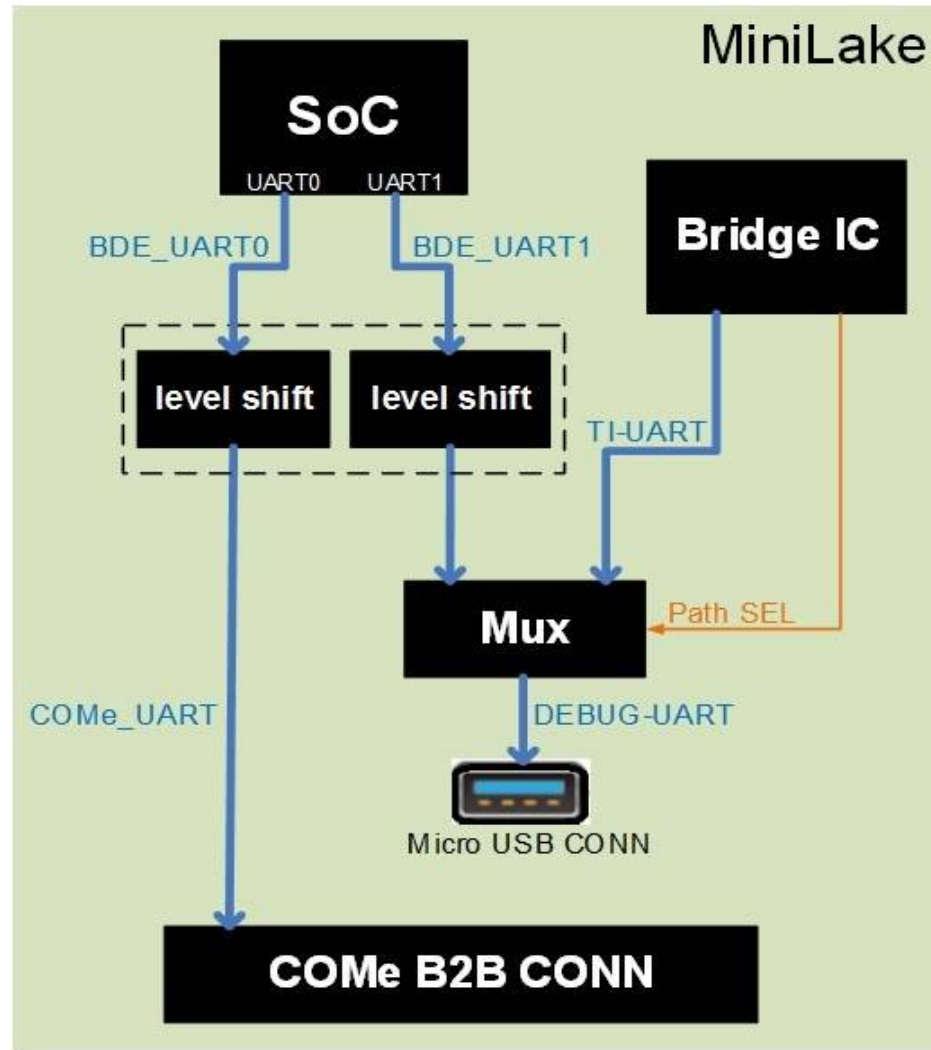


# *RESET BLOCK DIAGRAM*

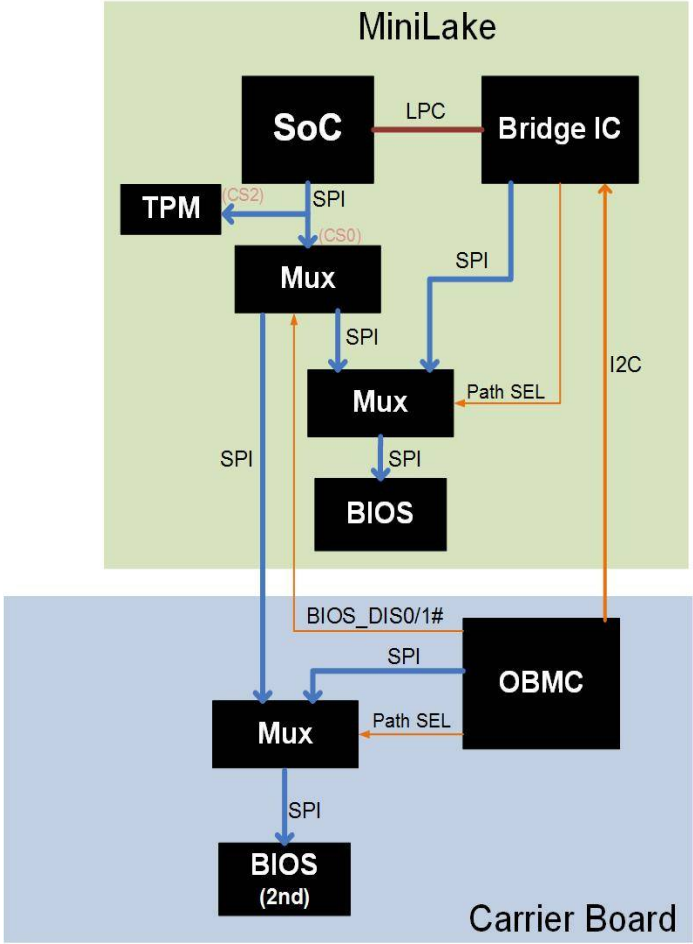
RESET BLOCK DIAGRAM



|            |          |                                 |                                |                |
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UART DIAGRAM



BLANK

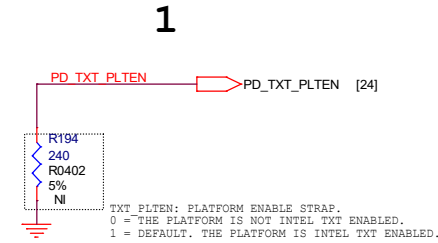
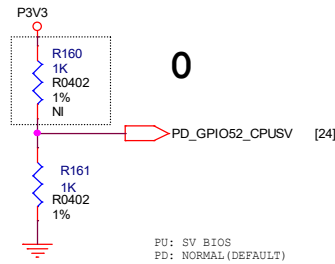
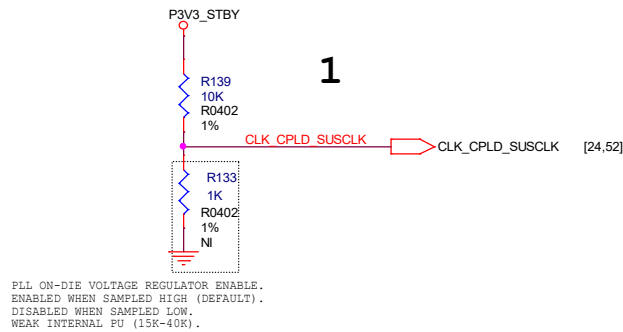


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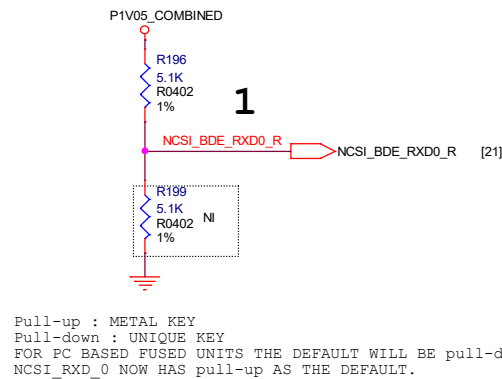
## GPIO62

## GP52\_GSXSLOAD

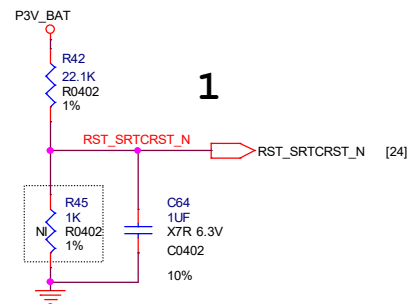
## TXT\_PLTEN



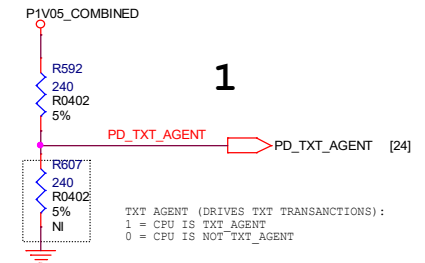
## NCSI\_RXD\_0



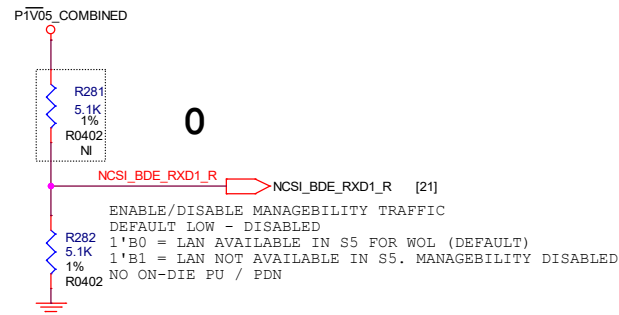
## CLEAR TPM REGISTERS



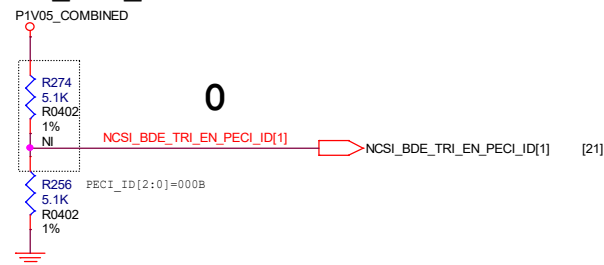
## TXT\_AGENT



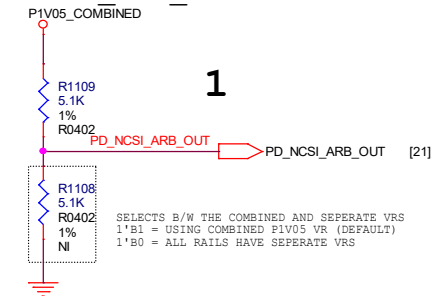
## NCSI\_RXD\_1



## NCSI\_TRI\_EN



## NCSI\_ARB\_OUT



## BDE STRAPPING\_1

Quanta

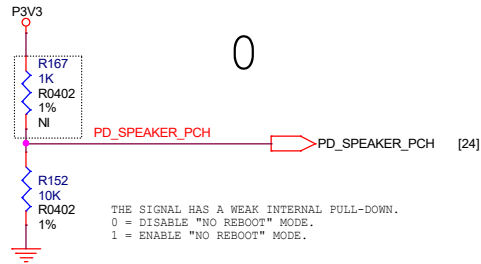
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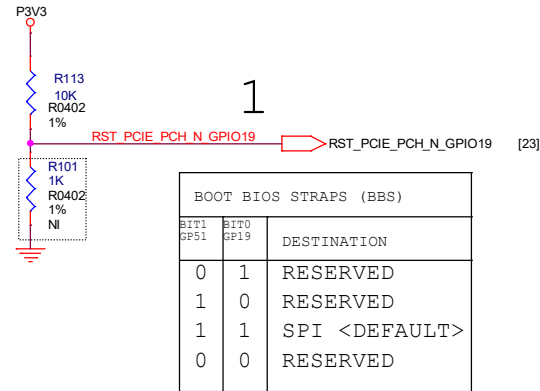
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Page Title BDE STRAPPING\_1Rev  
0.0

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## SPKR

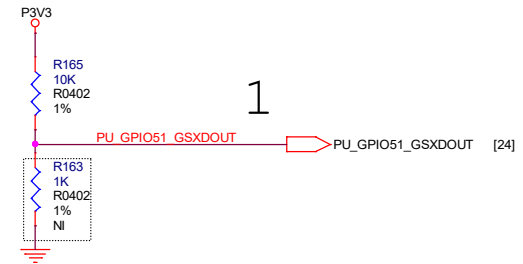


## GPIO19

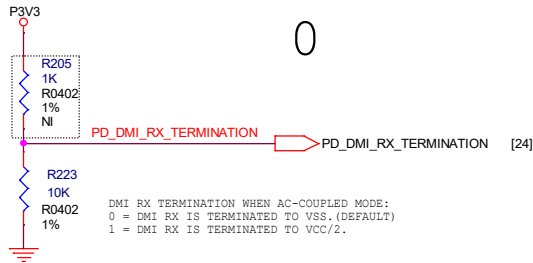


DESIGN NOTE: INTERNAL PULL-UP (15K-40K). DISABLED AFTER PLTRST# DEASSERTS.

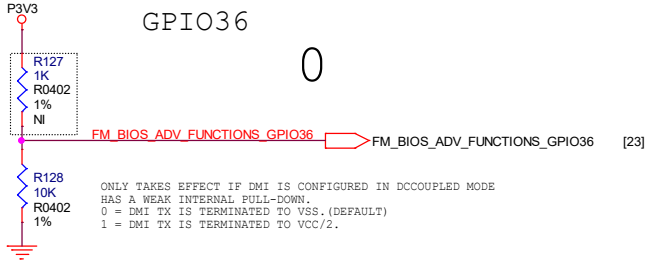
## GPIO51



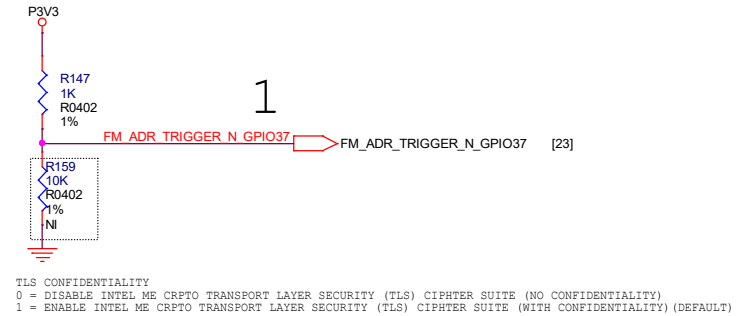
## GPIO33



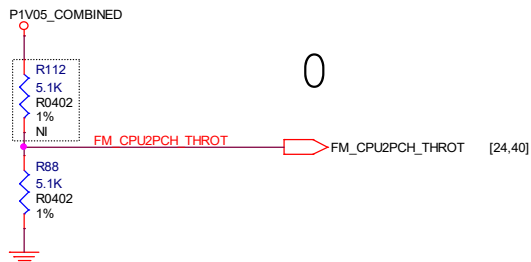
## BIOS\_ADV\_FUNCTIONS



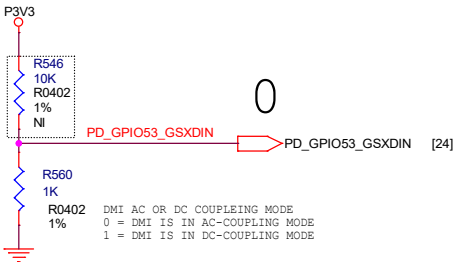
## GPIO37



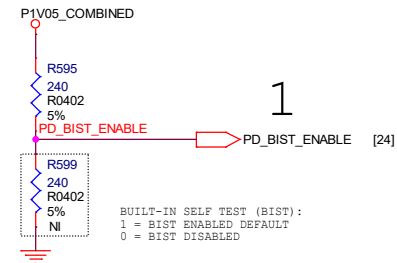
## CPU2PCH\_THROT



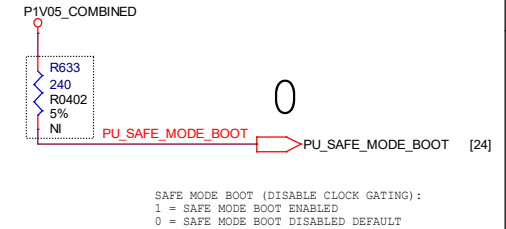
## GP53\_GSXDIN



## BIST\_ENABLE

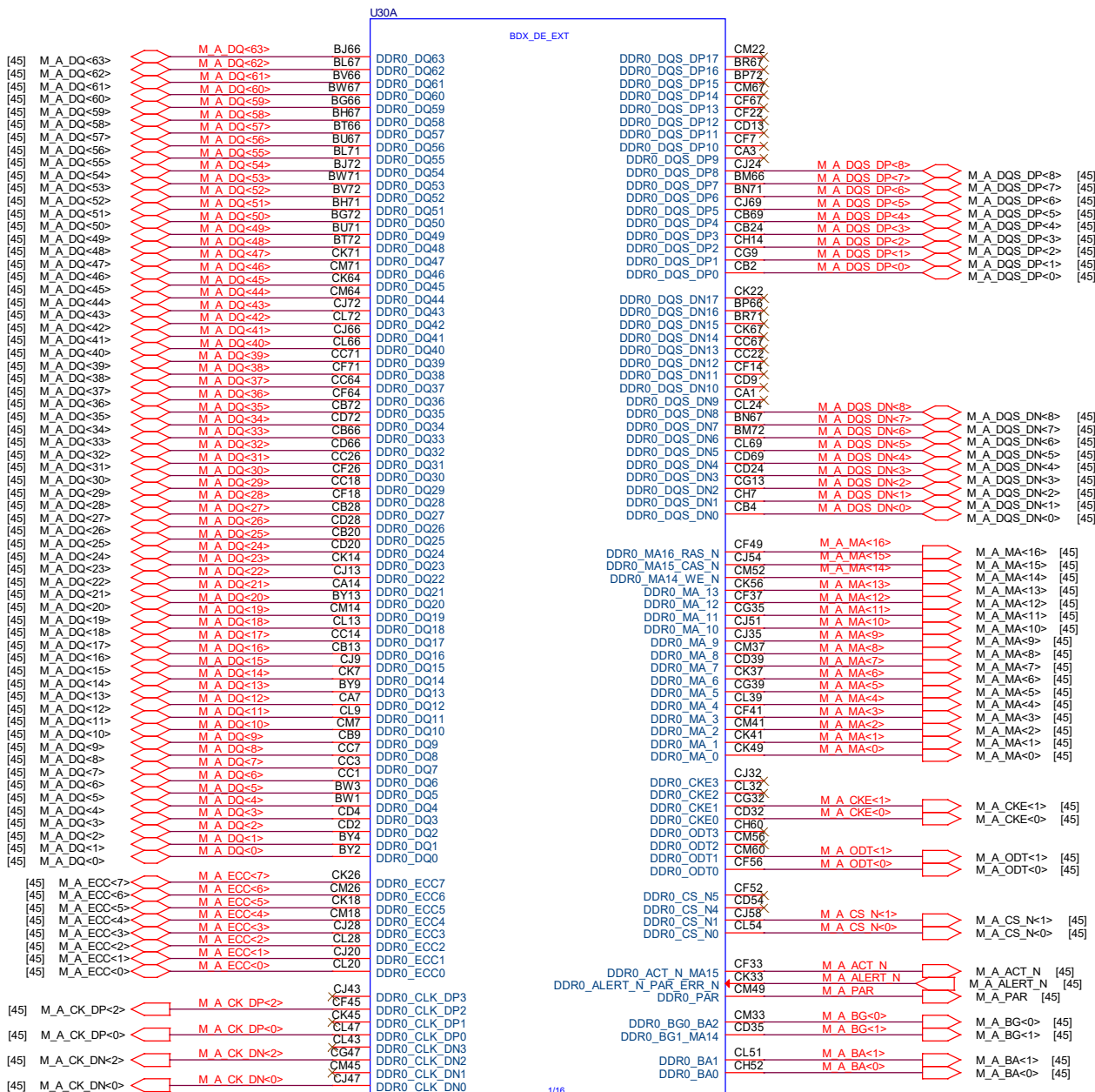


## SAFE\_MODE\_BOOT



Note : BIST\_ENABLE has internal pull-up to P1V05\_COMBINED.

DESIGN NOTE :  
The default setting should be checked for each board build

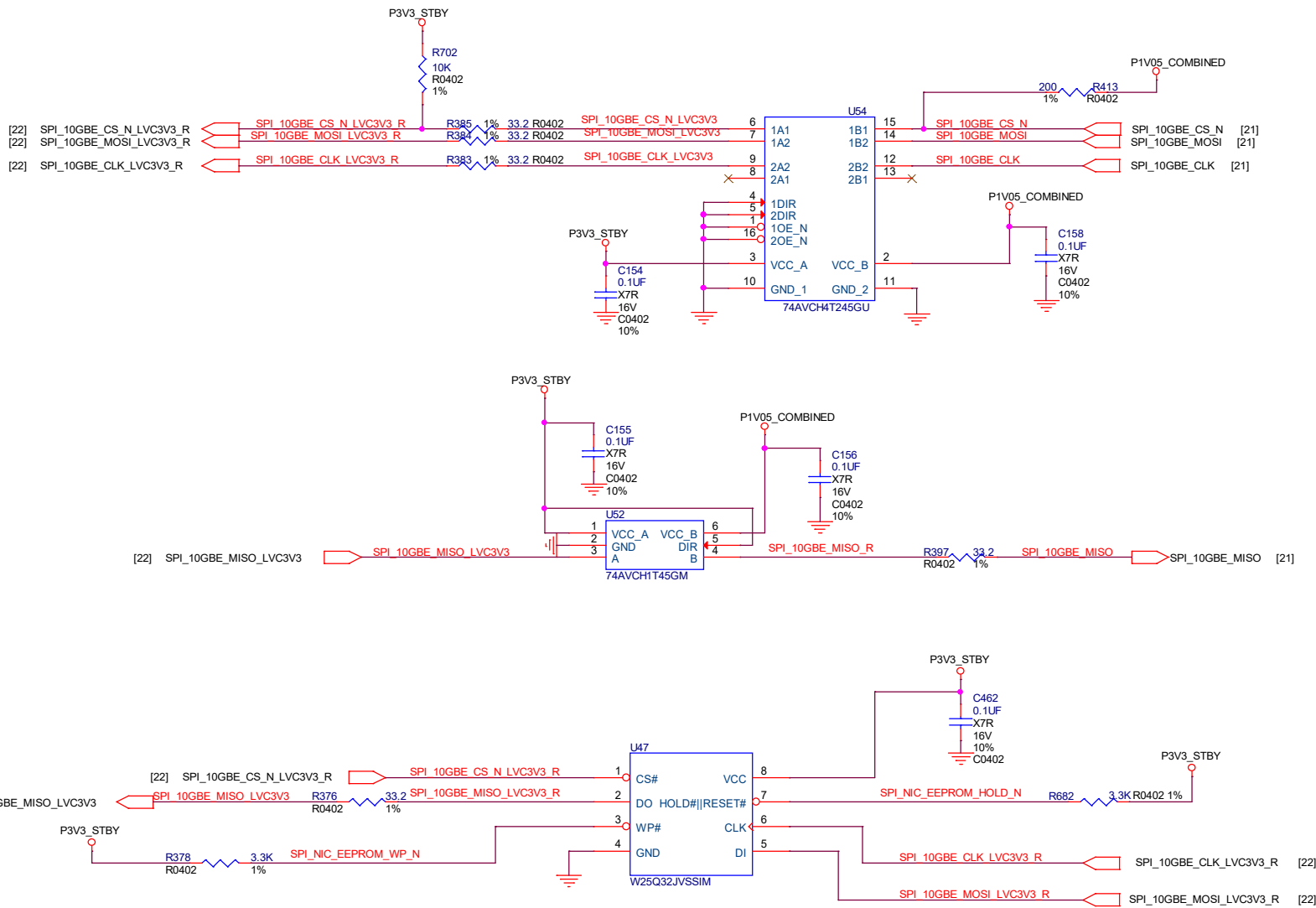


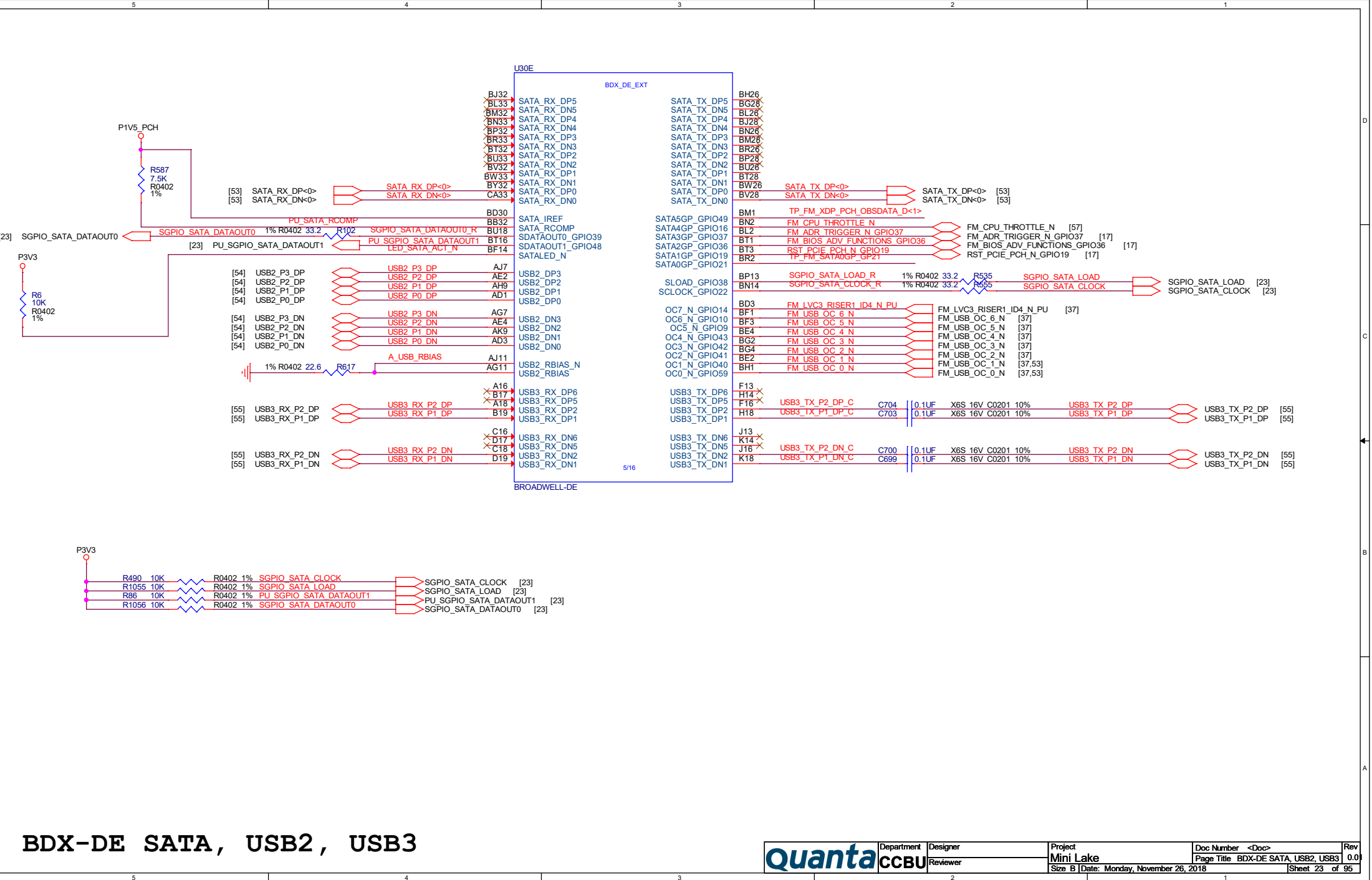
# BDX-DE DDR4 CHANNEL A



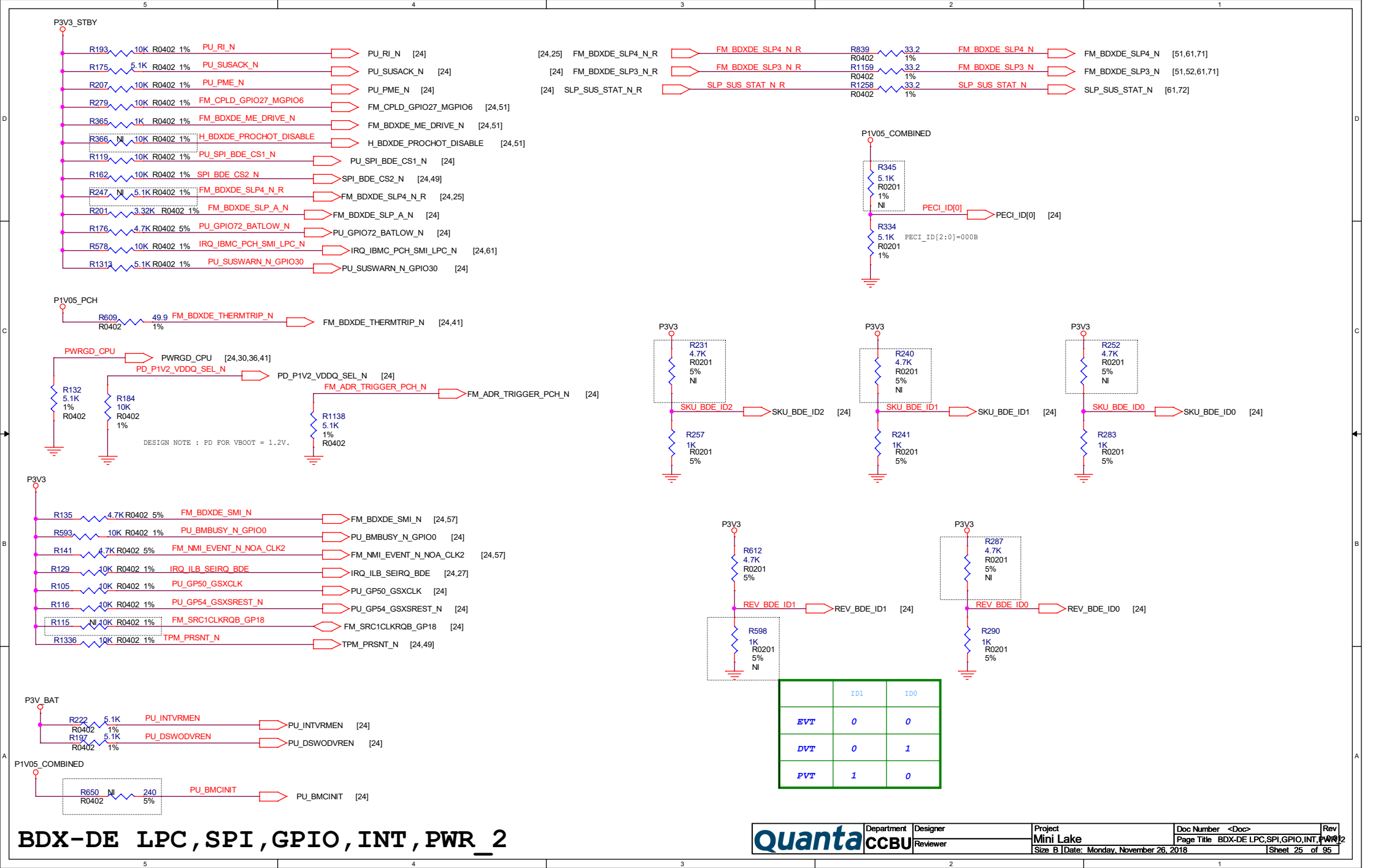












# BDX-DE LPC, SPI, GPIO, INT, PWR\_2

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Reviewer

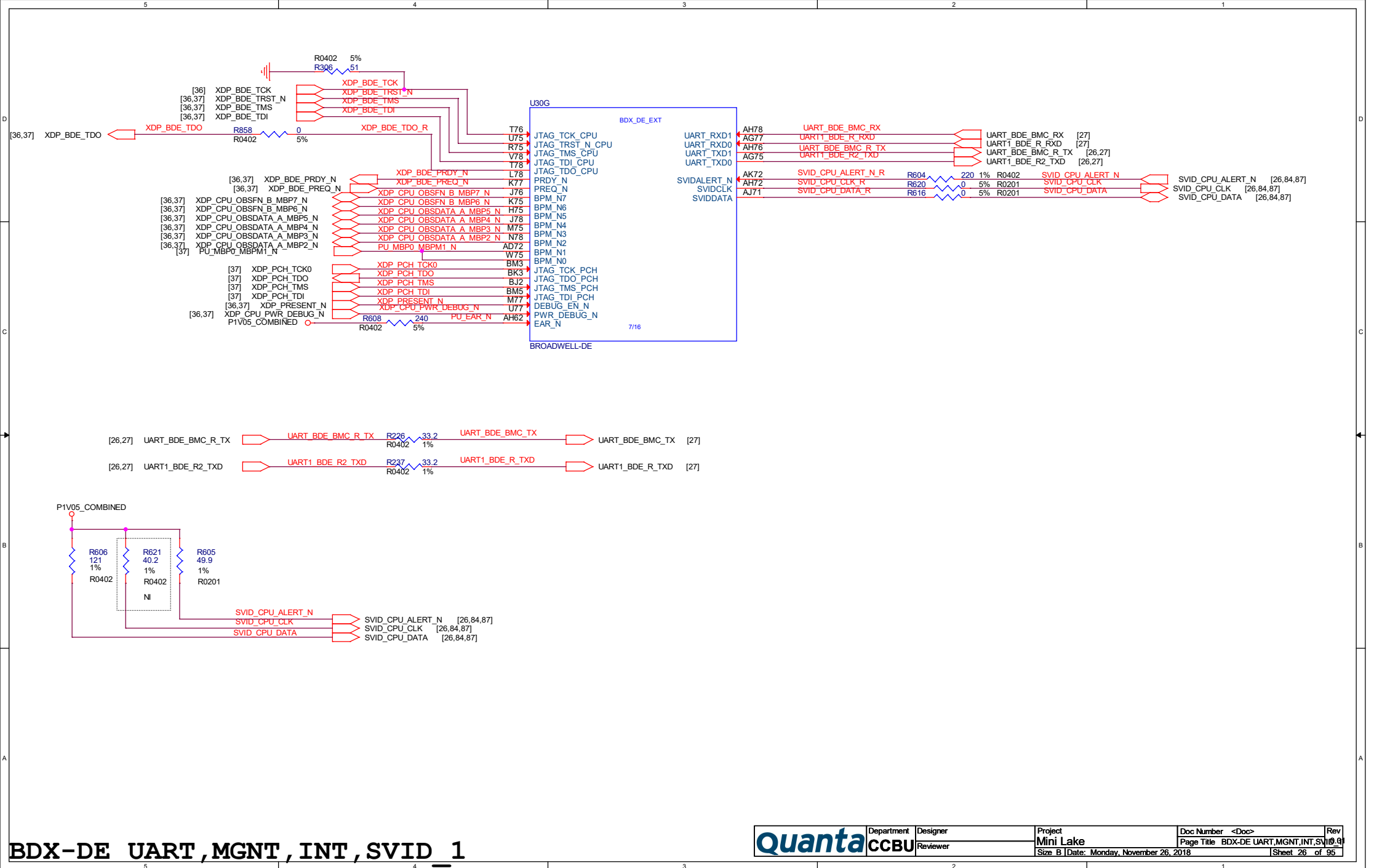
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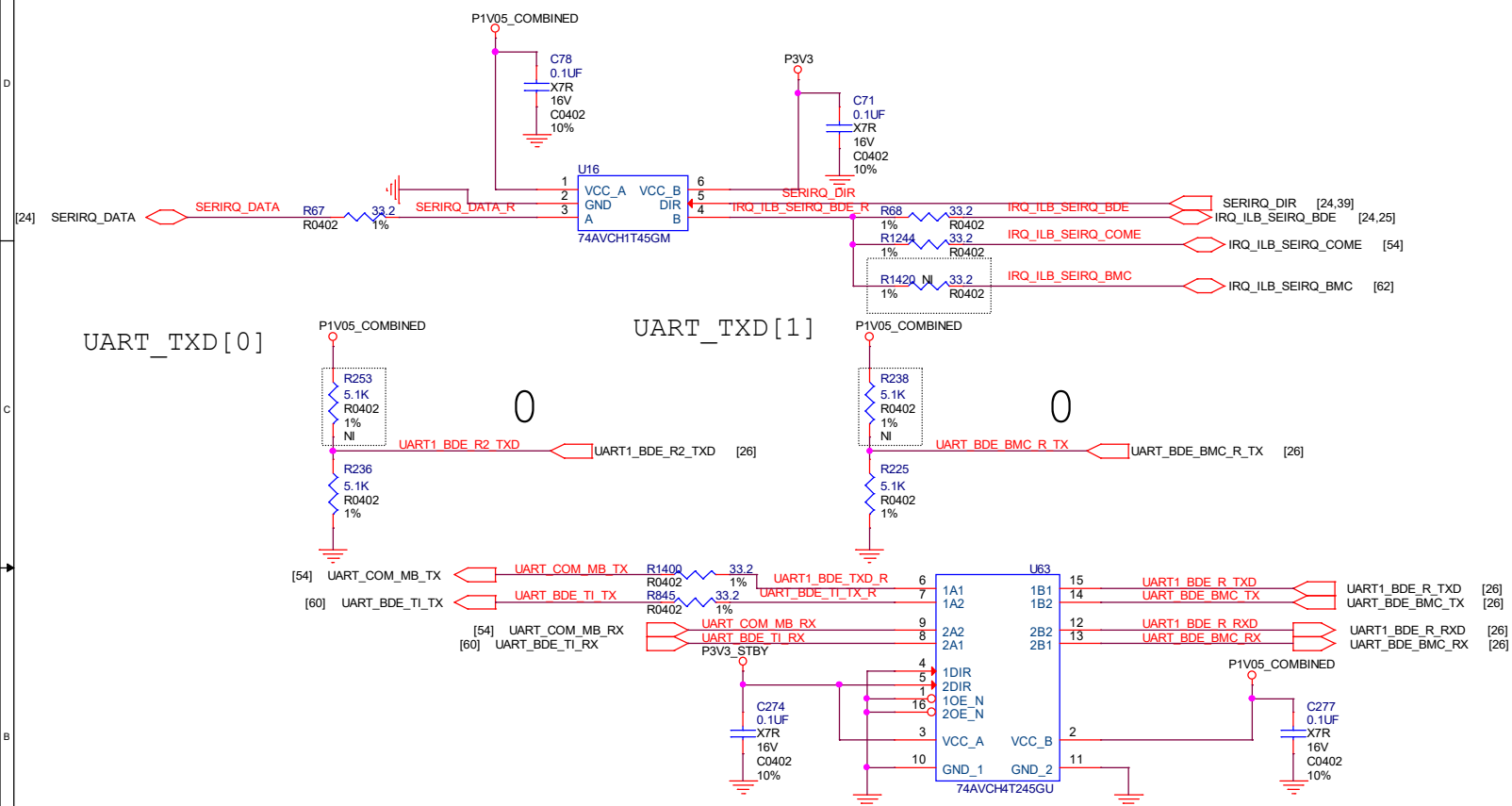
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BDX-DE LPC, SPI, GPIO, INT, PWR\_2

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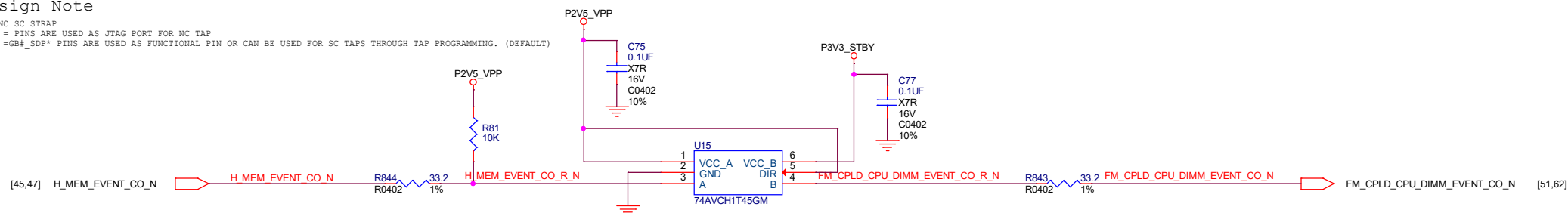


Need change to NXP and check CRB.  
CHECK THIS. SUPPORT VOLTAGE BEED TO 0.8 to 3.6V



## Design Note

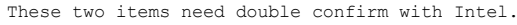
TAP\_NC\_SC\_STRAP  
1'B1 = PINS ARE USED AS JTAG PORT FOR NC TAP  
1'B0 =#B SDP\* PINS ARE USED AS FUNCTIONAL PIN OR CAN BE USED FOR SC TAPS THROUGH TAP PROGRAMMING. (DEFAULT)



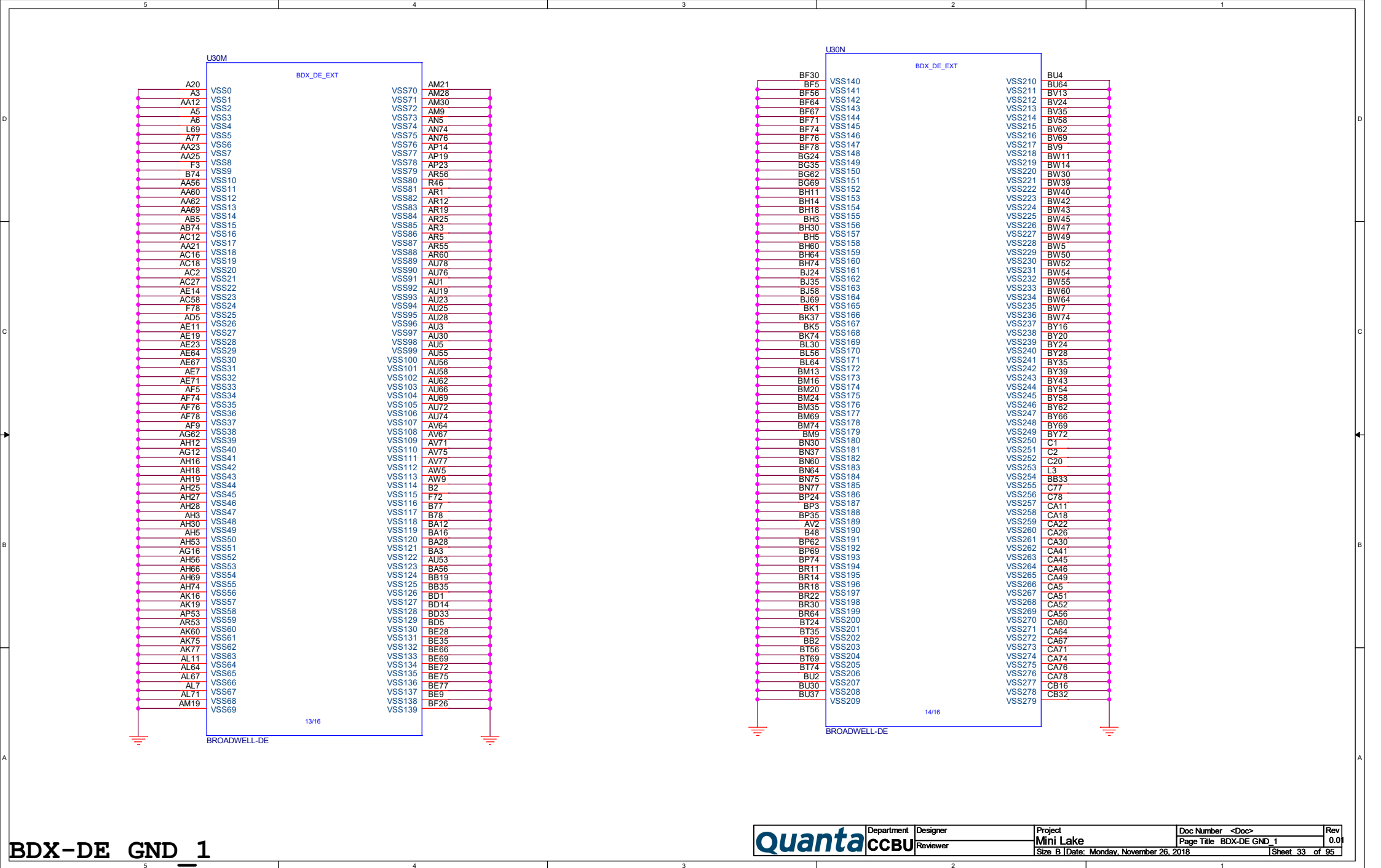


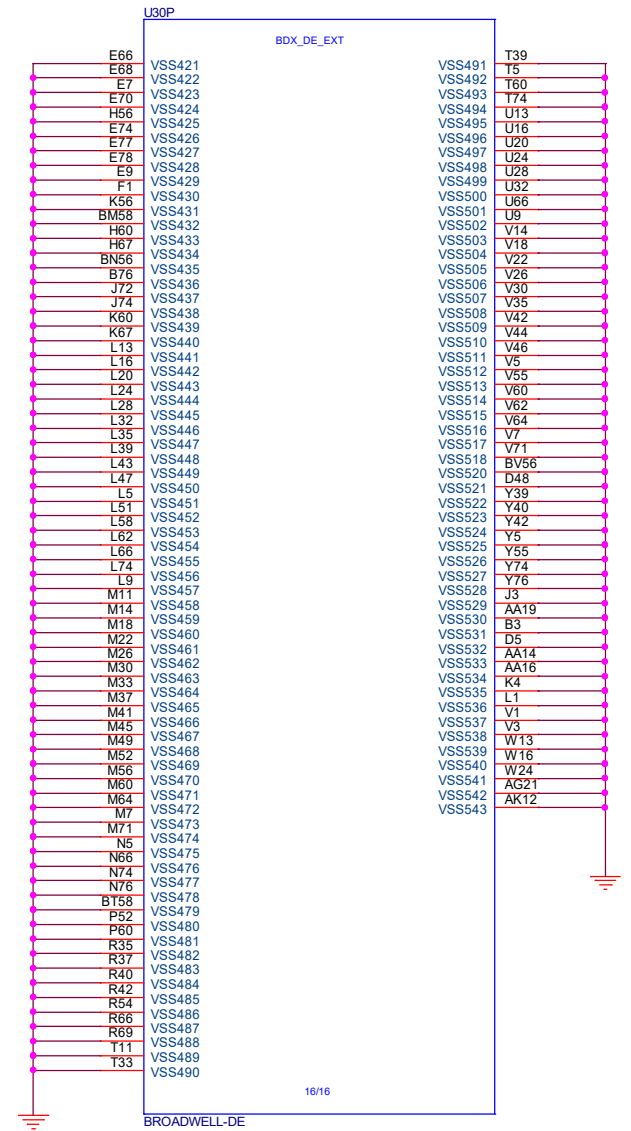
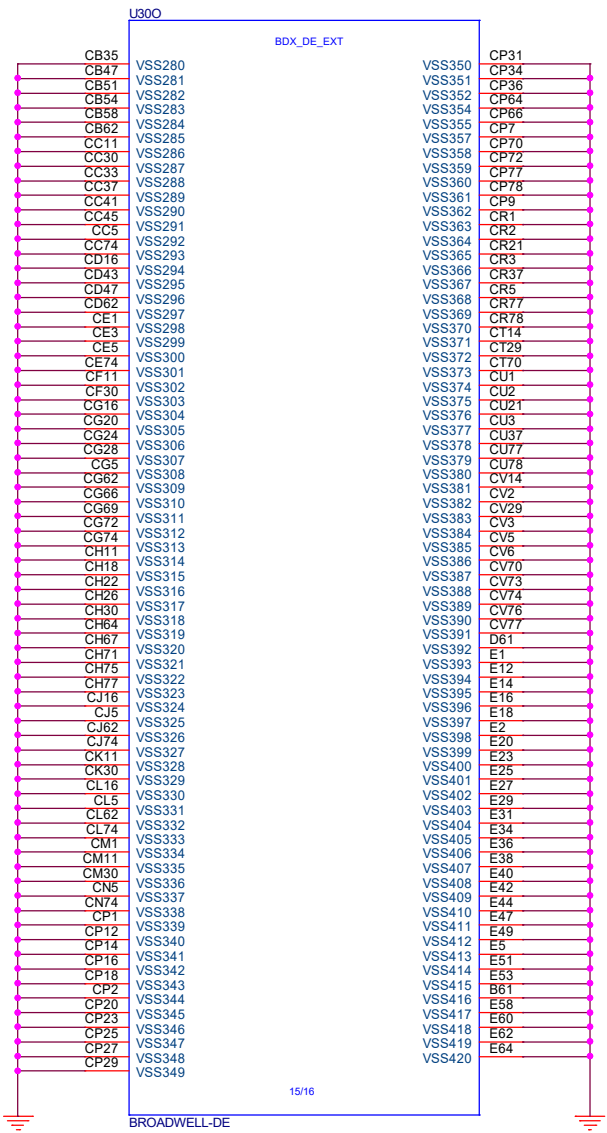










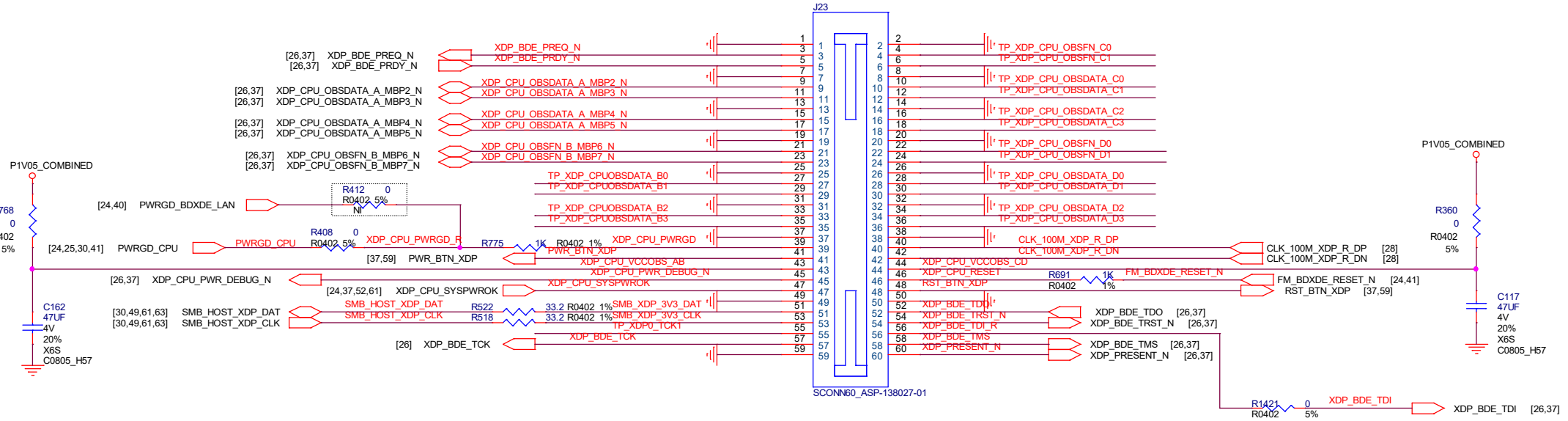


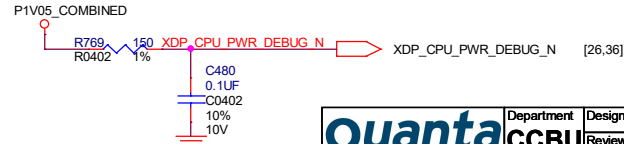
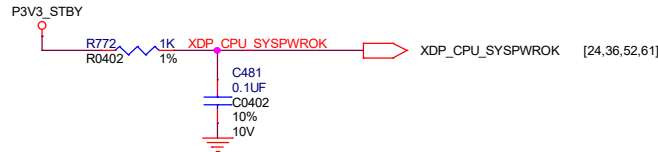
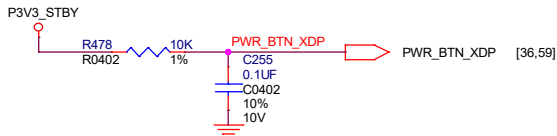
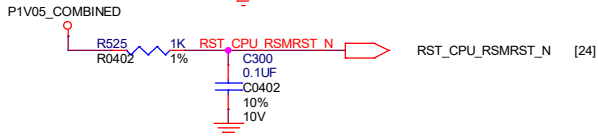
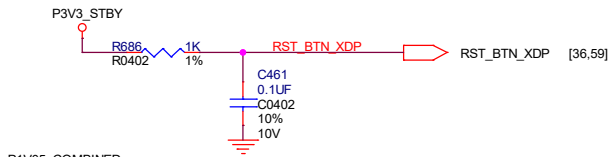
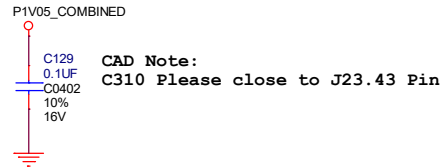
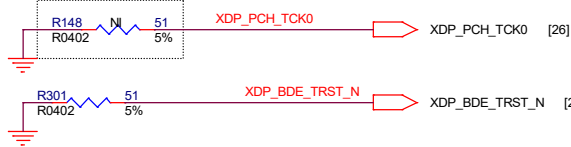
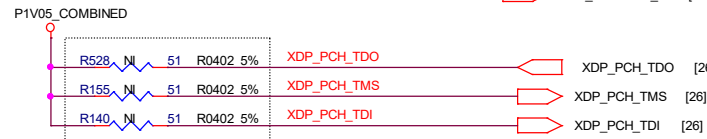
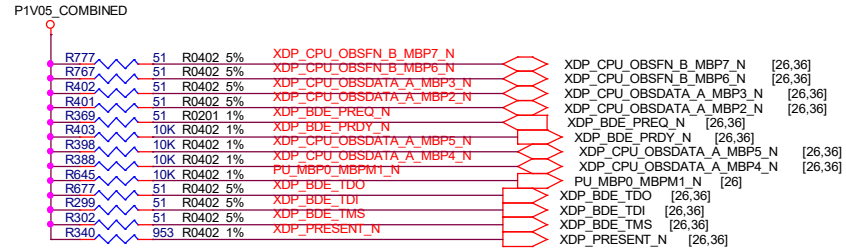
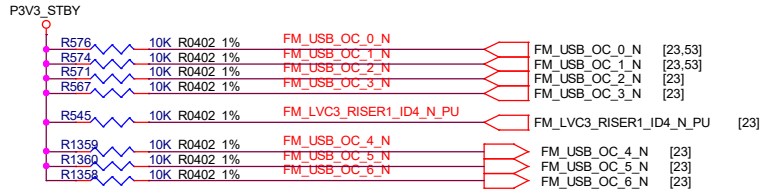
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# CPU XDP





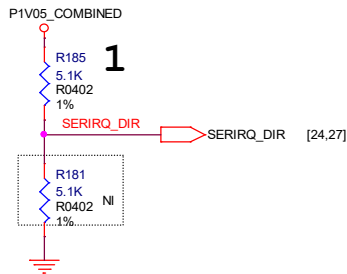
CPU\_XDP\_2

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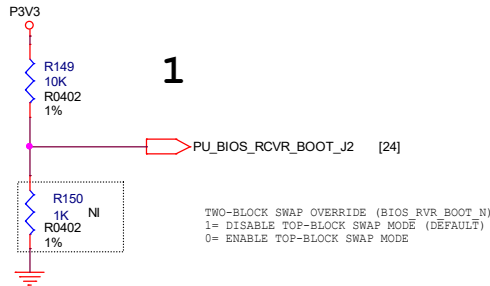


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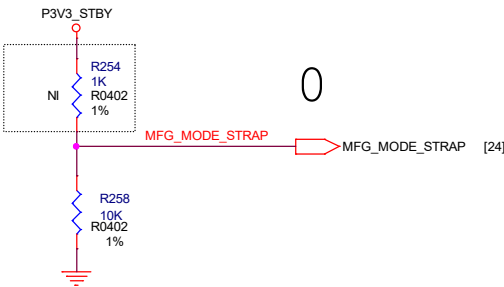
SERIRQ\_DIR



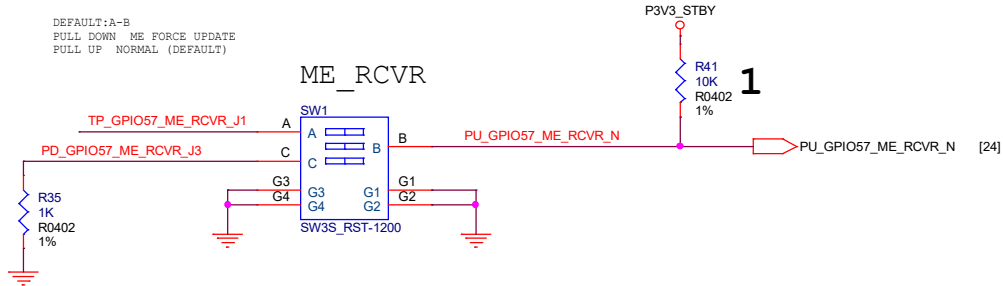
TOP\_BLOCK\_SWAP

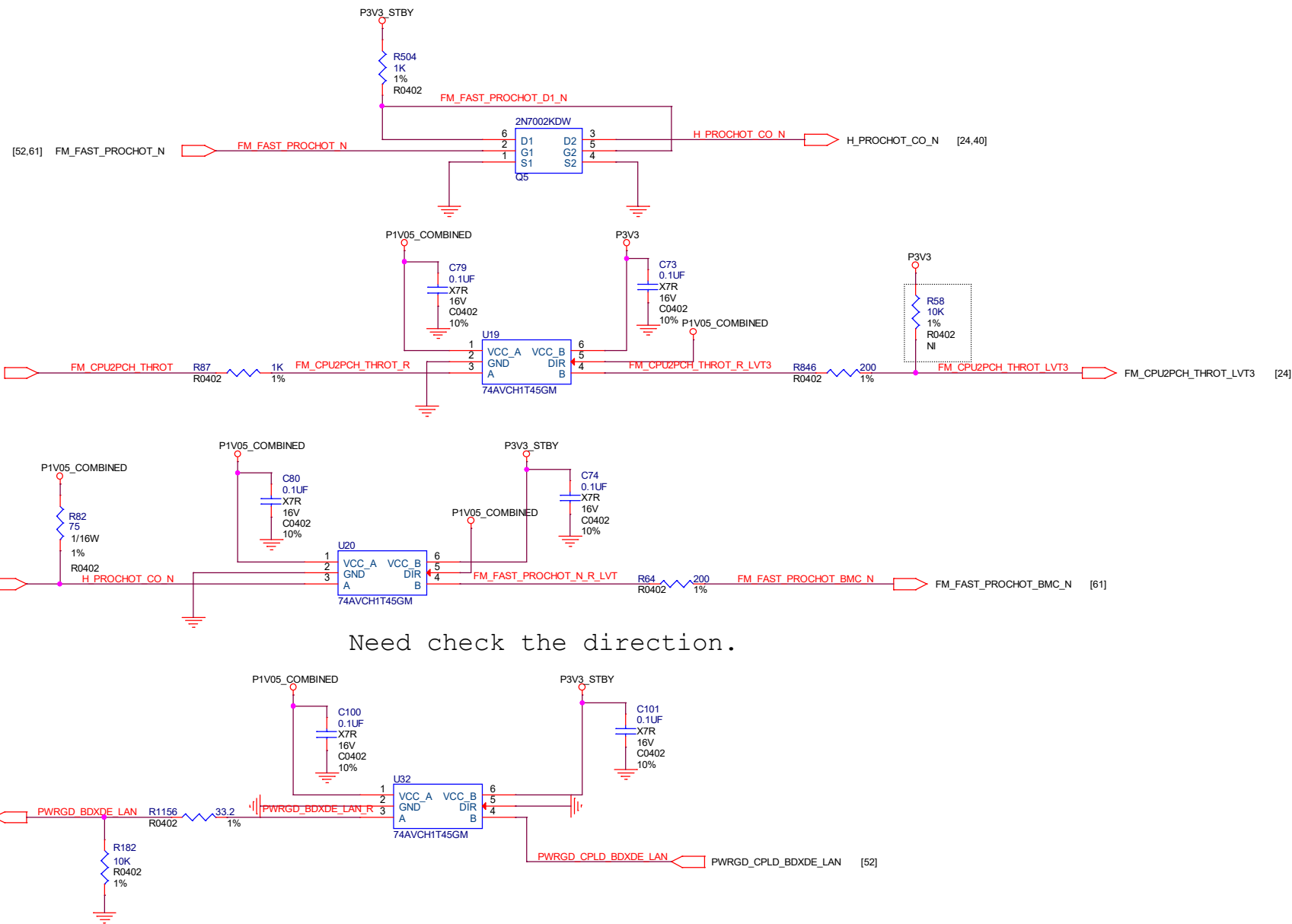


MFG\_MODE\_STRAP

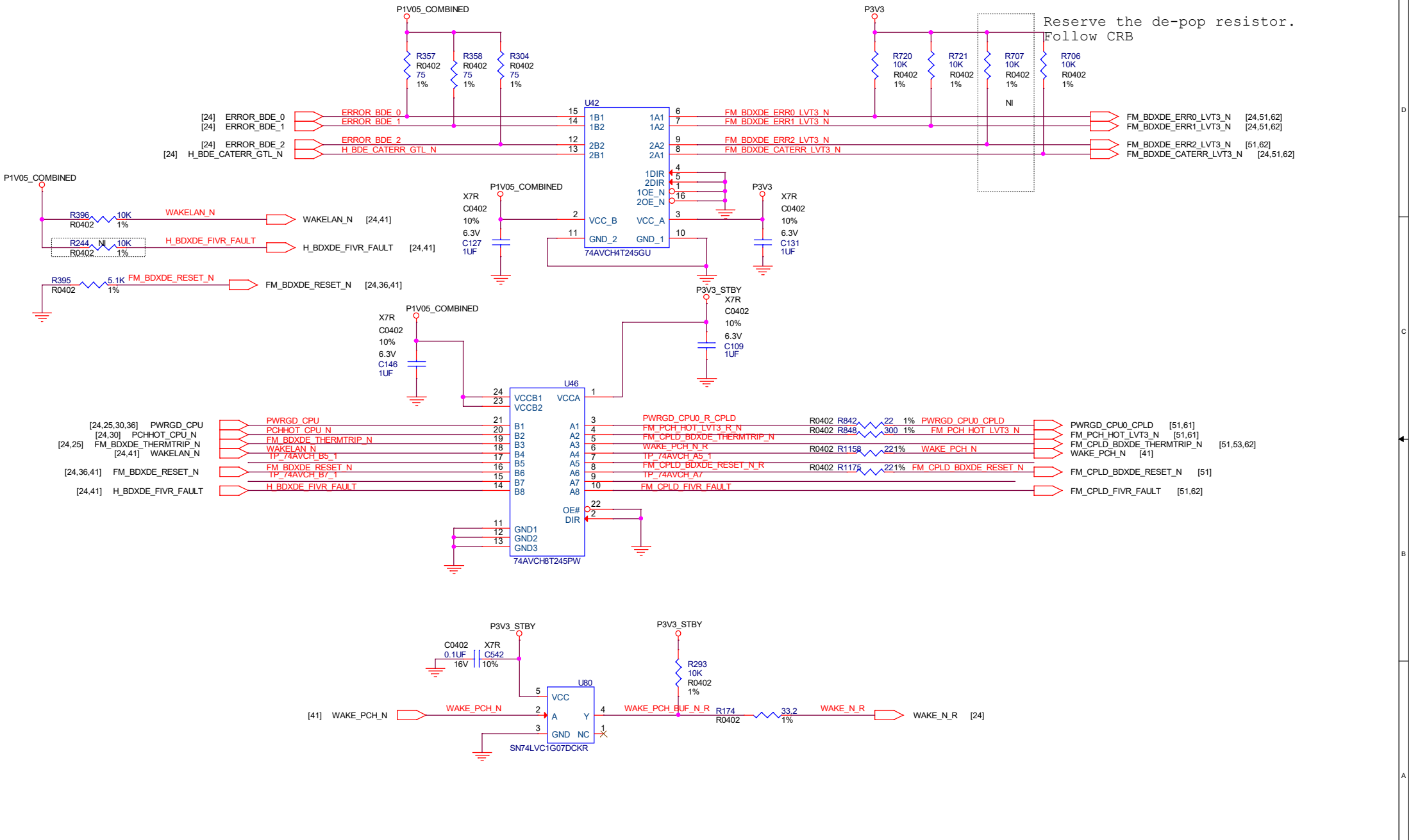


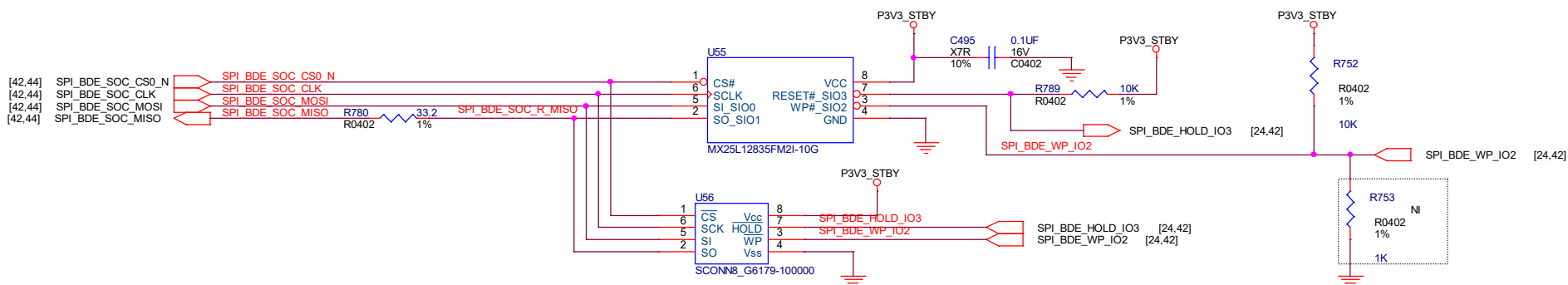
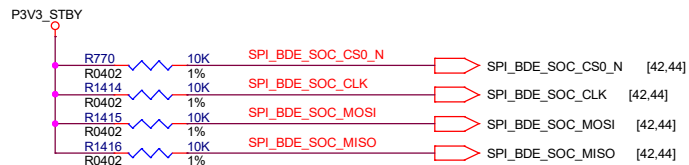
ME\_RCVR





# ERROR CNTL 1

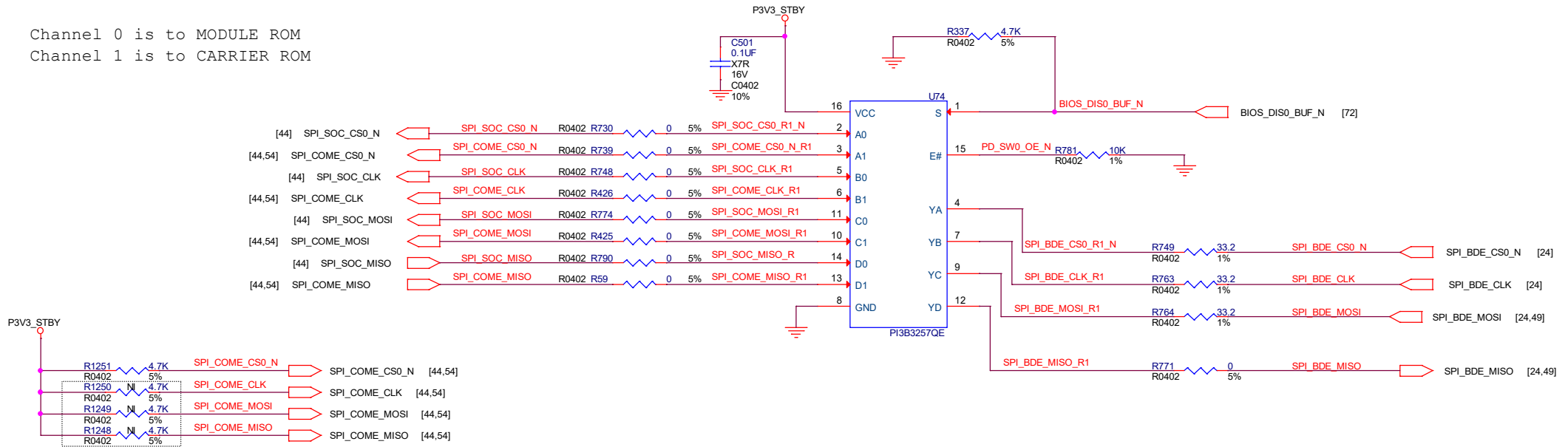




**CAD Note:**  
 THIS PART WILL CO-LAY WITH SOCKET  
 USE ALT SYMBOL ASSOCIATED WITH SOCKET FOOTPRINT

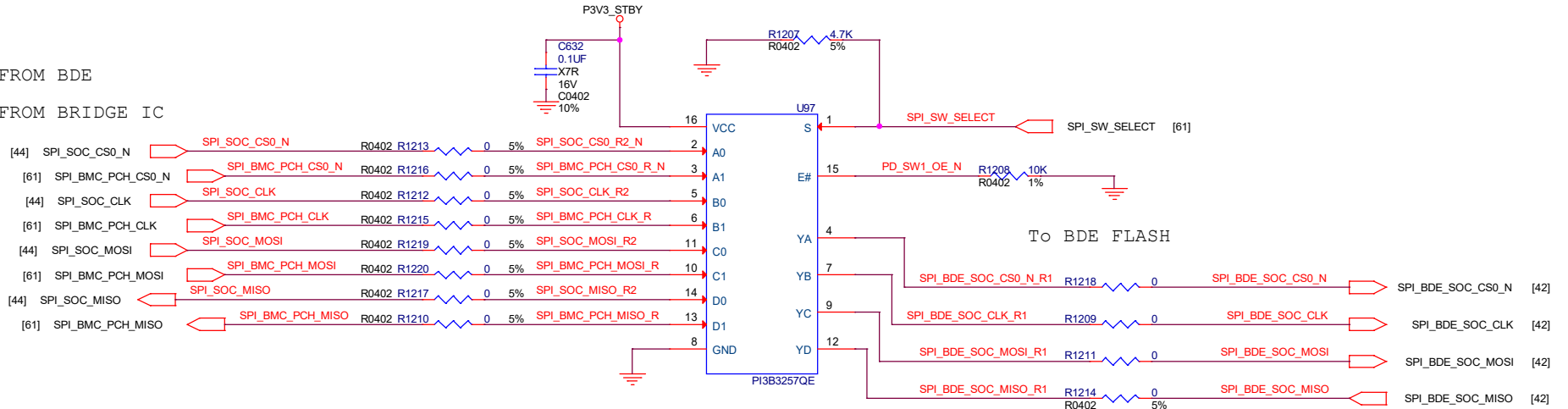


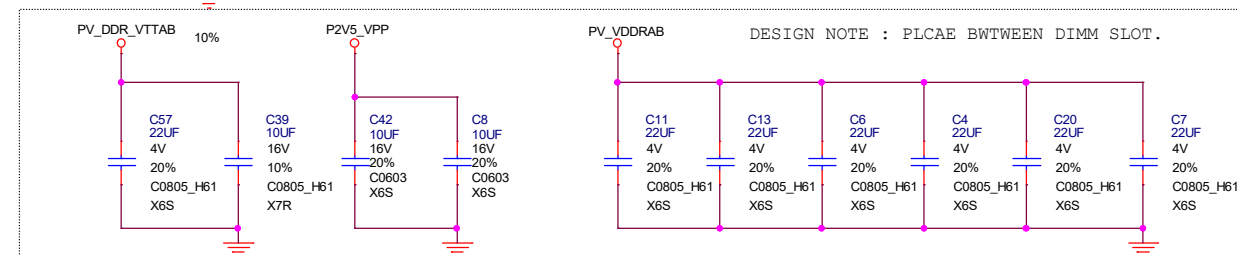
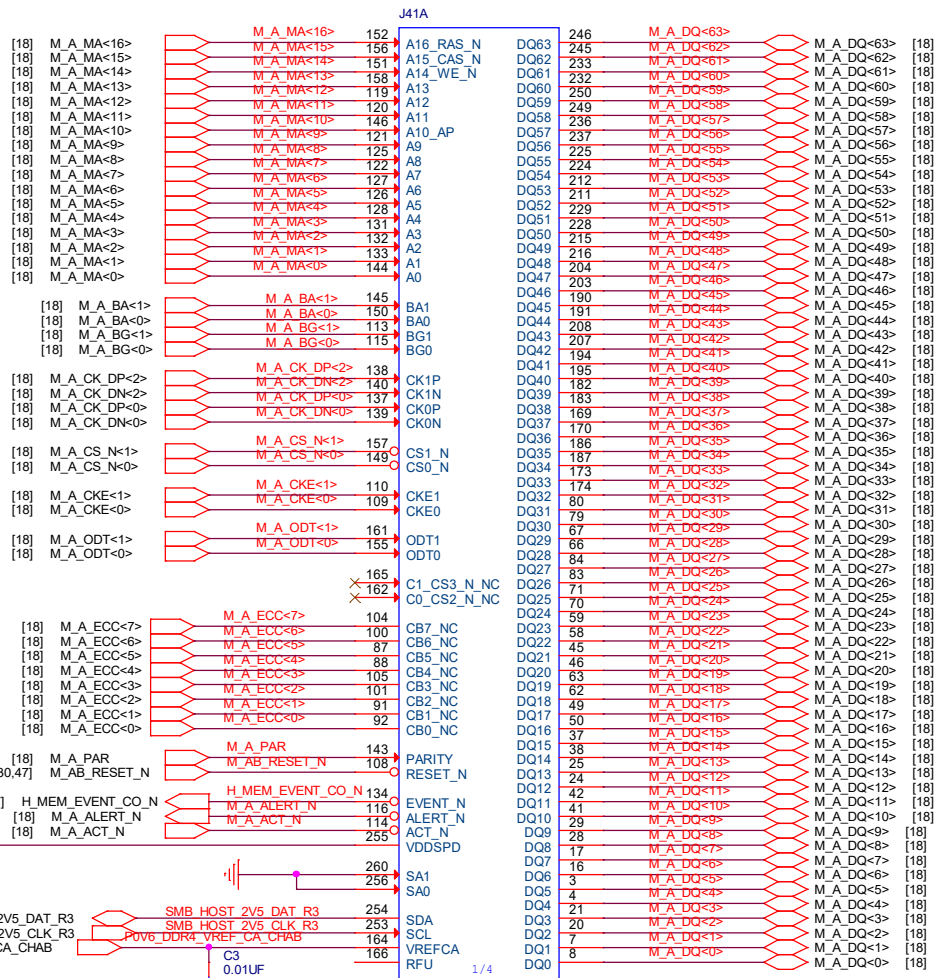
Channel 0 is to MODULE ROM  
Channel 1 is to CARRIER ROM



Channel 0 FROM BDE

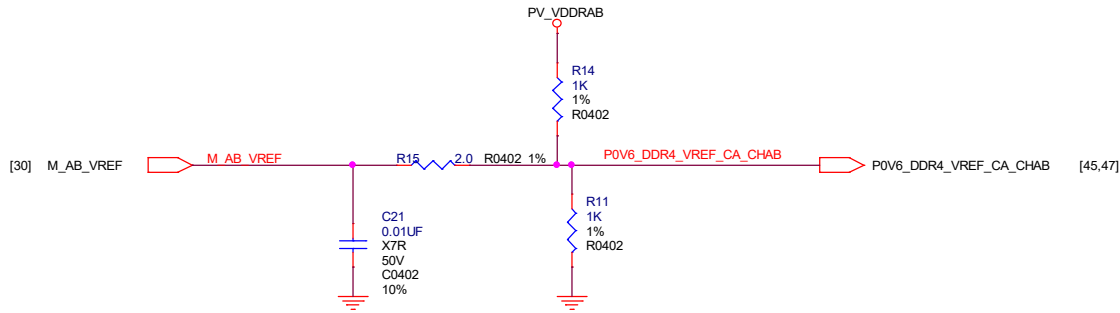
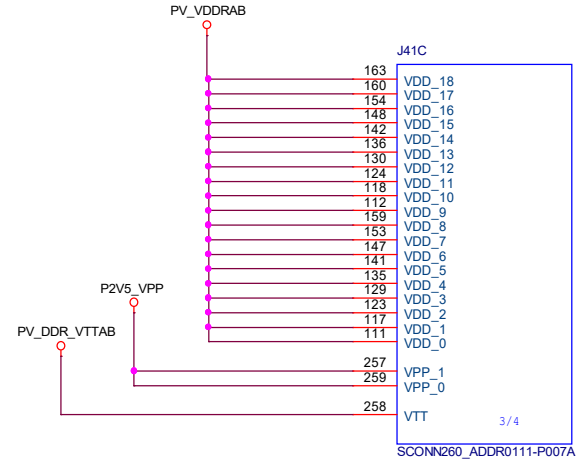
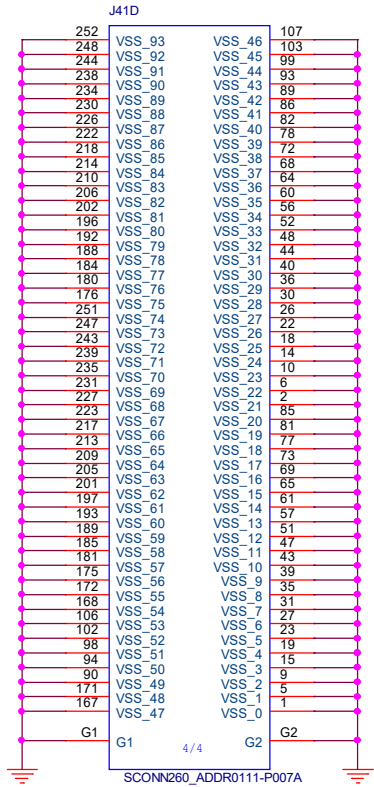
Channel 1 FROM BRIDGE IC

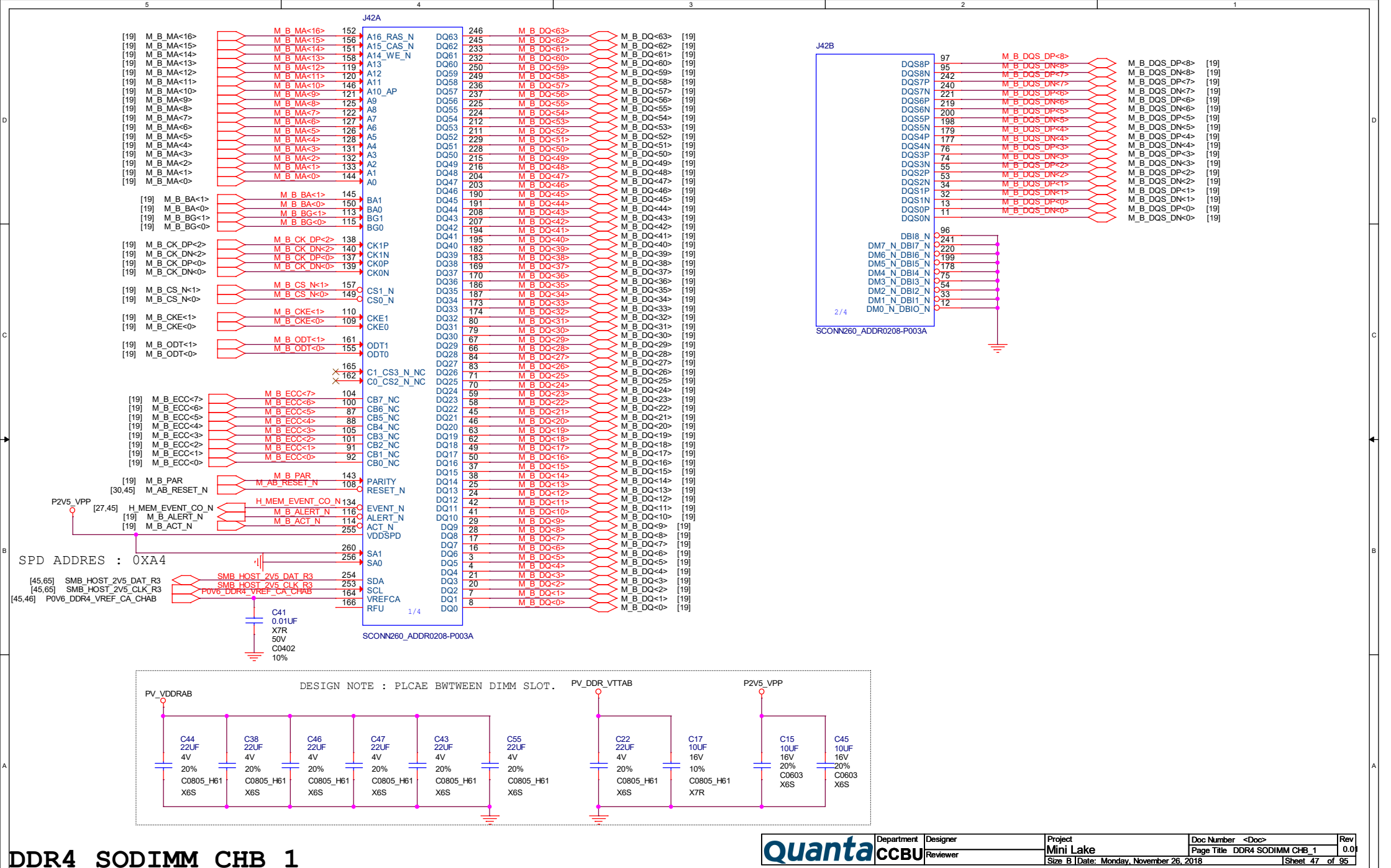


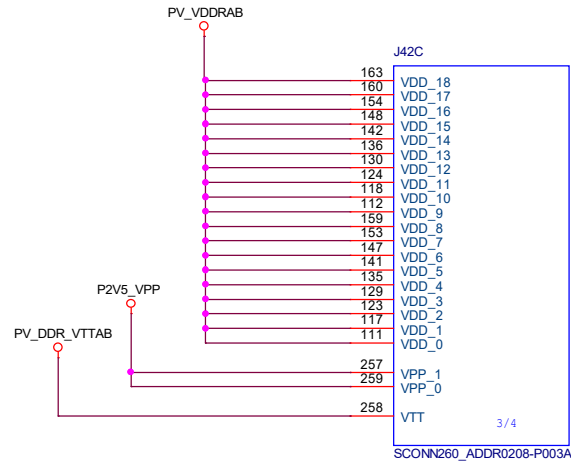
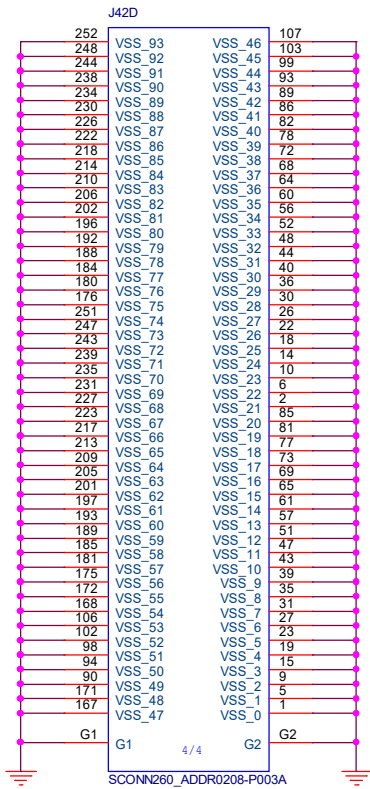


SPD ADDRES : 0XA0

# DDR4 SODIMM CHA 1







|               |             |          |           |                                 |                |
|---------------|-------------|----------|-----------|---------------------------------|----------------|
| <b>Quanta</b> | Department  | Designer | Project   | Doc Number <Doc>                | Rev            |
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Department  
CCBU

Designer  
Reviewer

Project  
Mini Lake

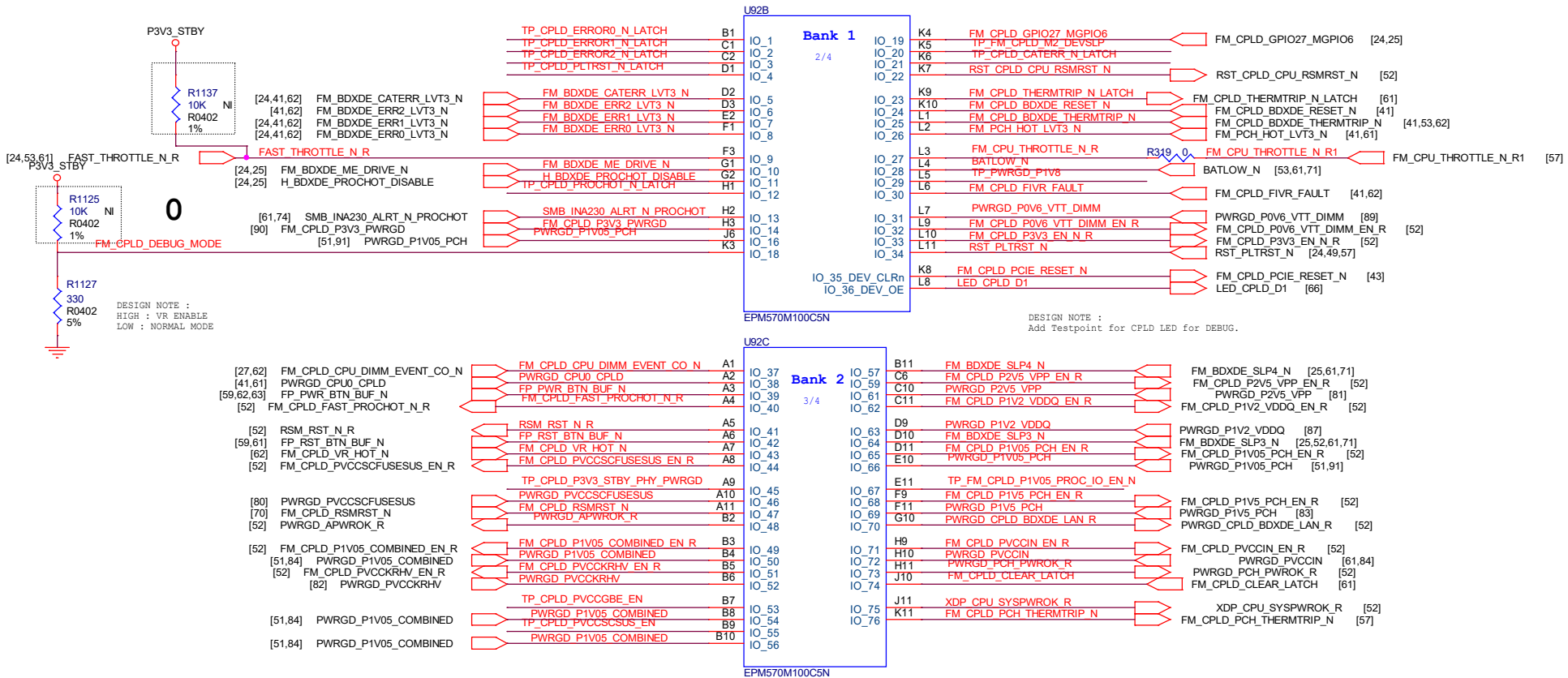
Doc Number <Doc>  
Page Title BLANK

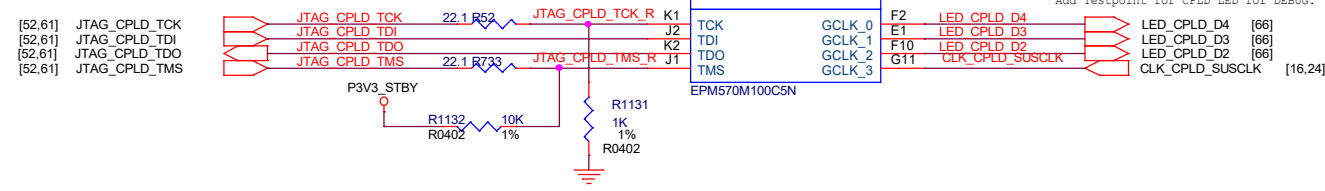
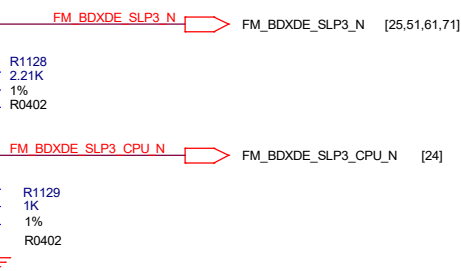
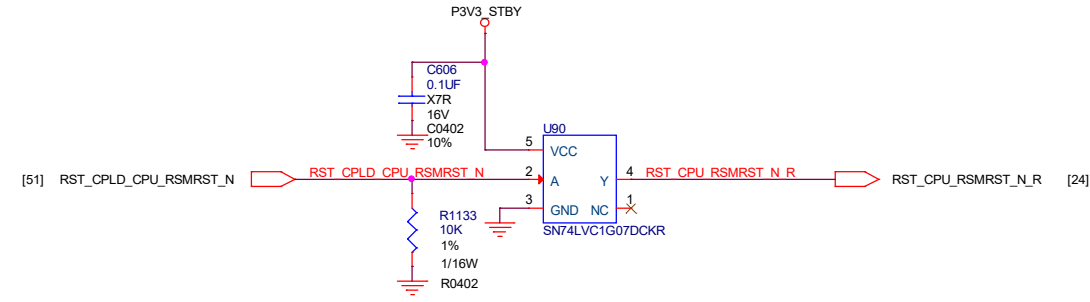
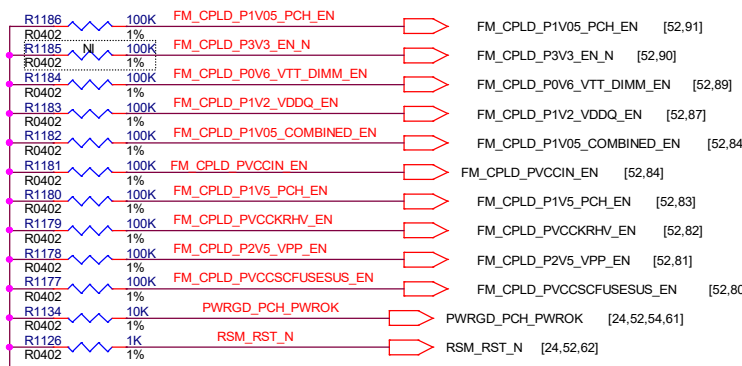
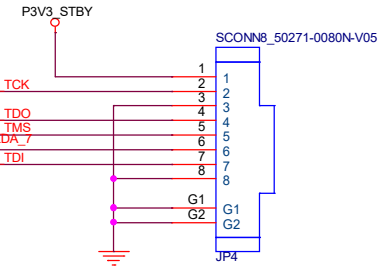
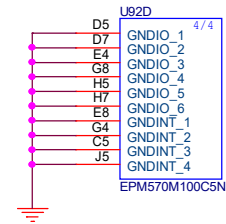
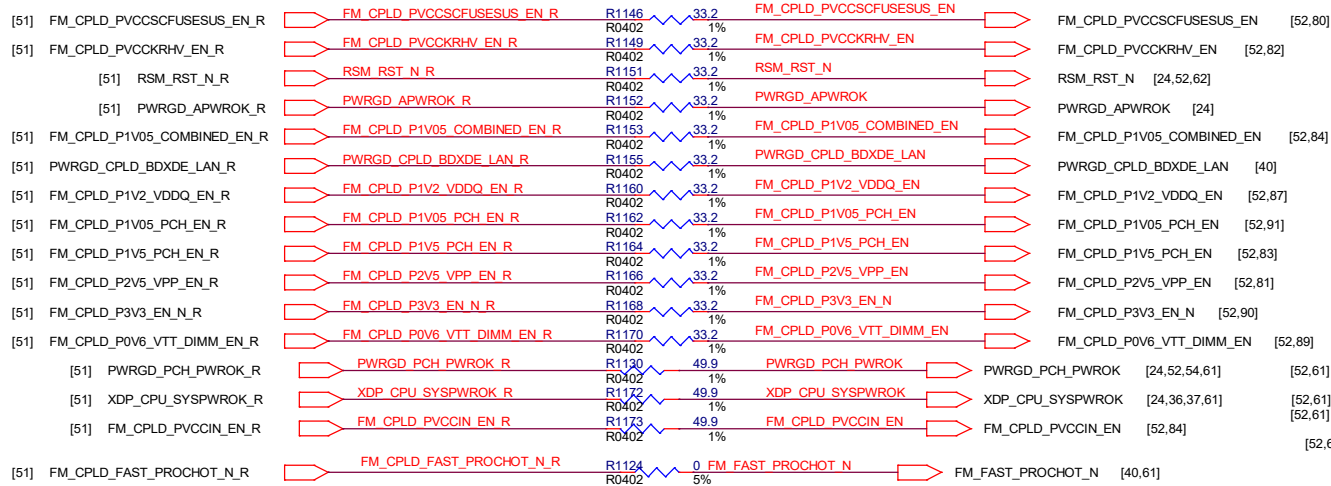
Rev  
0.0

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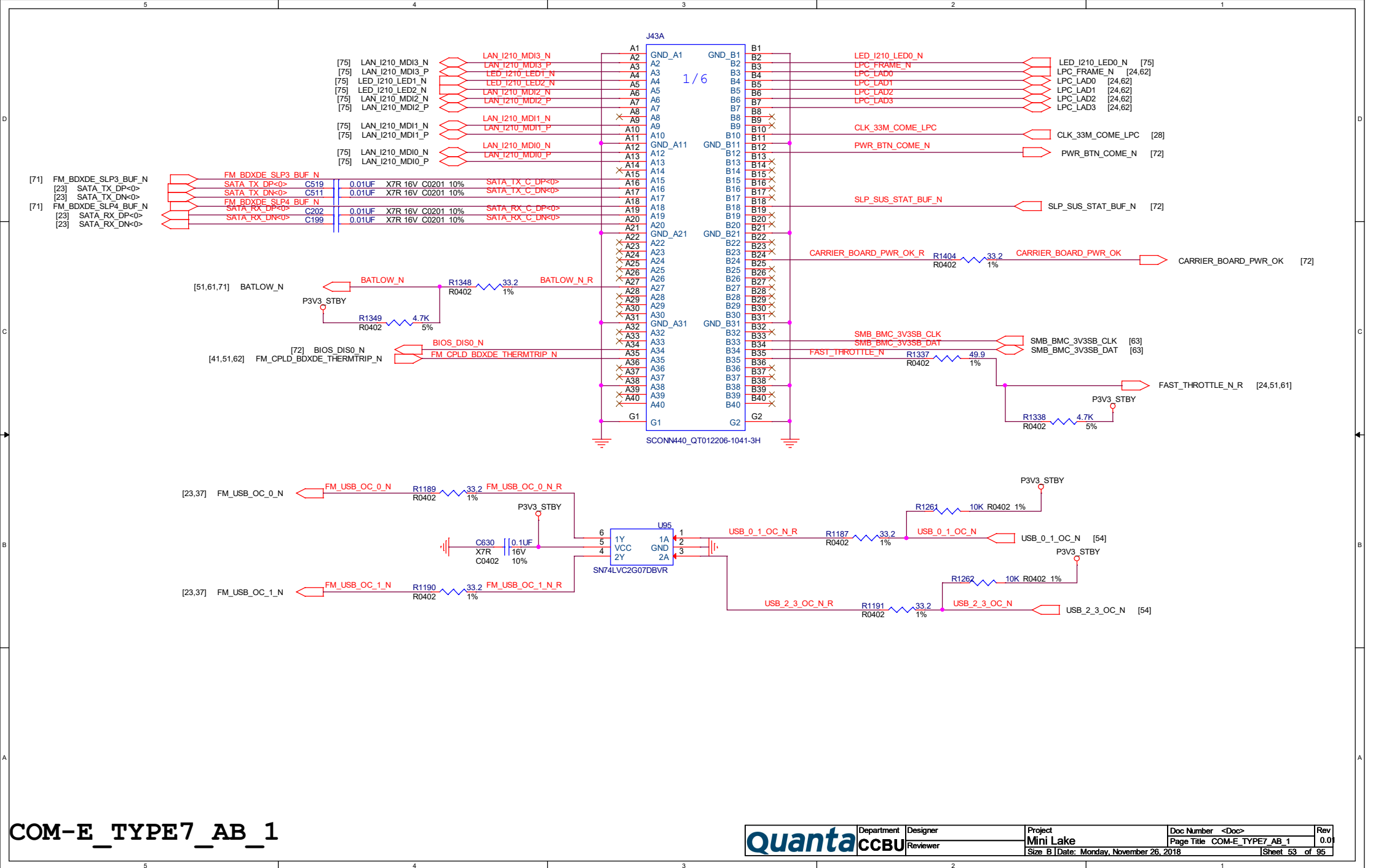
DESIGN NOTE :  
Below latch signals are useless.  
Will left to non-connect.

FM\_CPLD\_CATERR\_N\_LATCH  
FM\_CPLD\_CLEAR\_LATCH  
FM\_CPLD\_ERROR0\_N\_LATCH  
FM\_CPLD\_ERROR1\_N\_LATCH  
FM\_CPLD\_ERROR2\_N\_LATCH  
FM\_CPLD\_FCHHOT\_N\_GP74\_LATCH  
FM\_CPLD\_PLTRST\_N\_LATCH  
FM\_CPLD\_PROCHOT\_N\_LATCH  
FM\_CPLD\_THERMTRIP\_N\_LATCH





DESIGN NOTE :  
Add Testpoint for CPLD LED for DEBUG.



COM-E\_TYPE7\_AB\_1

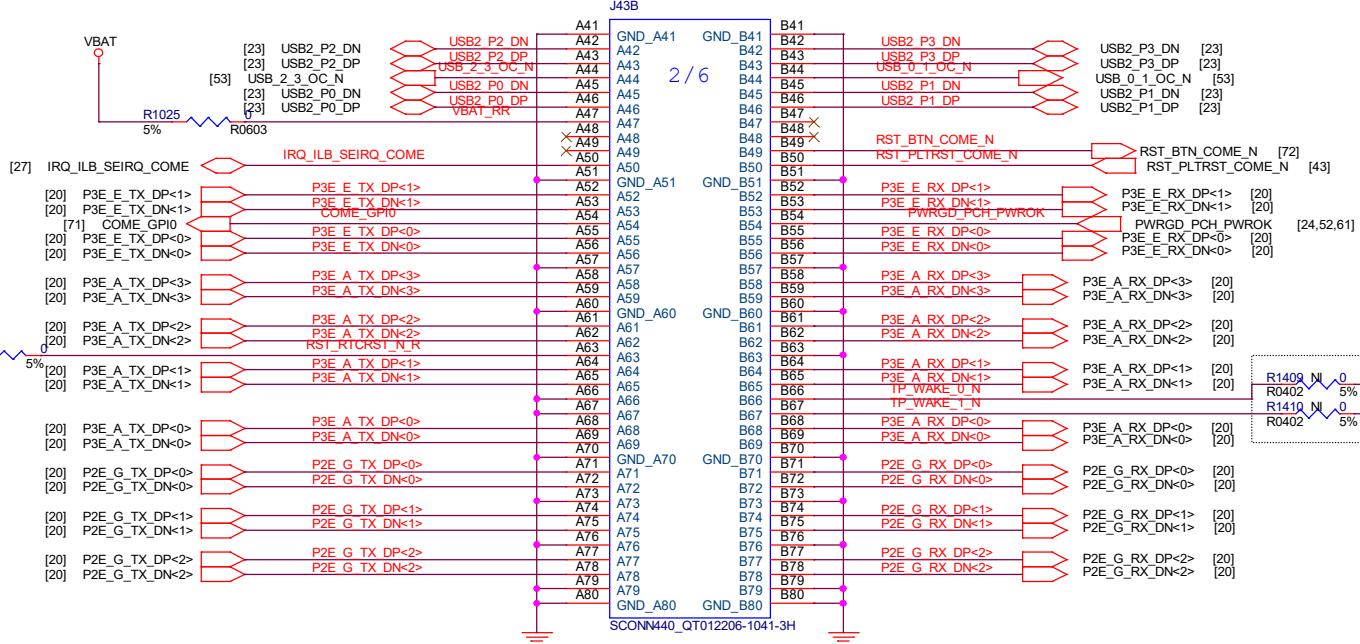
CMOS CLEAR

[24] RST\_RTCRST\_N

RST\_RTCRST\_N



1



[20] P2E\_G\_TX\_DP<3>  
[20] P2E\_G\_TX\_DN<3>

P2E\_G\_TX\_DP<3>  
P2E\_G\_TX\_DN<3>

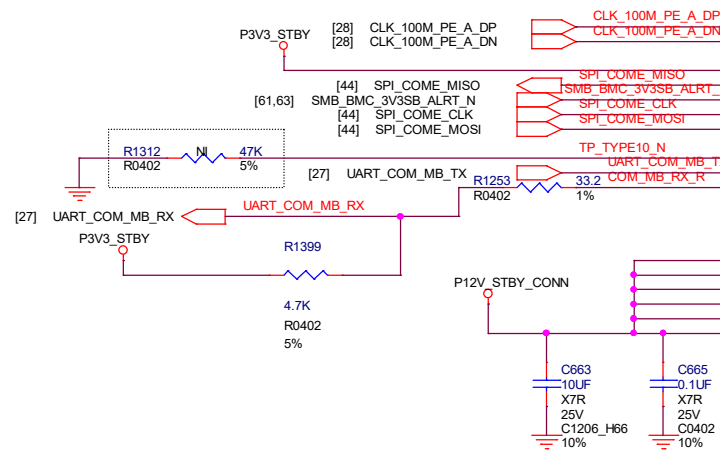
J43C

3 / 6

P2E\_G\_RX\_DP<3>  
P2E\_G\_RX\_DN<3>

P2E\_G\_RX\_DP<3>  
P2E\_G\_RX\_DN<3>

[20] P5V\_STBY



COM-E TYPE7 AB 2

Quanta

Department CCBU

Designer

Reviewer

Project Mini Lake

Size B

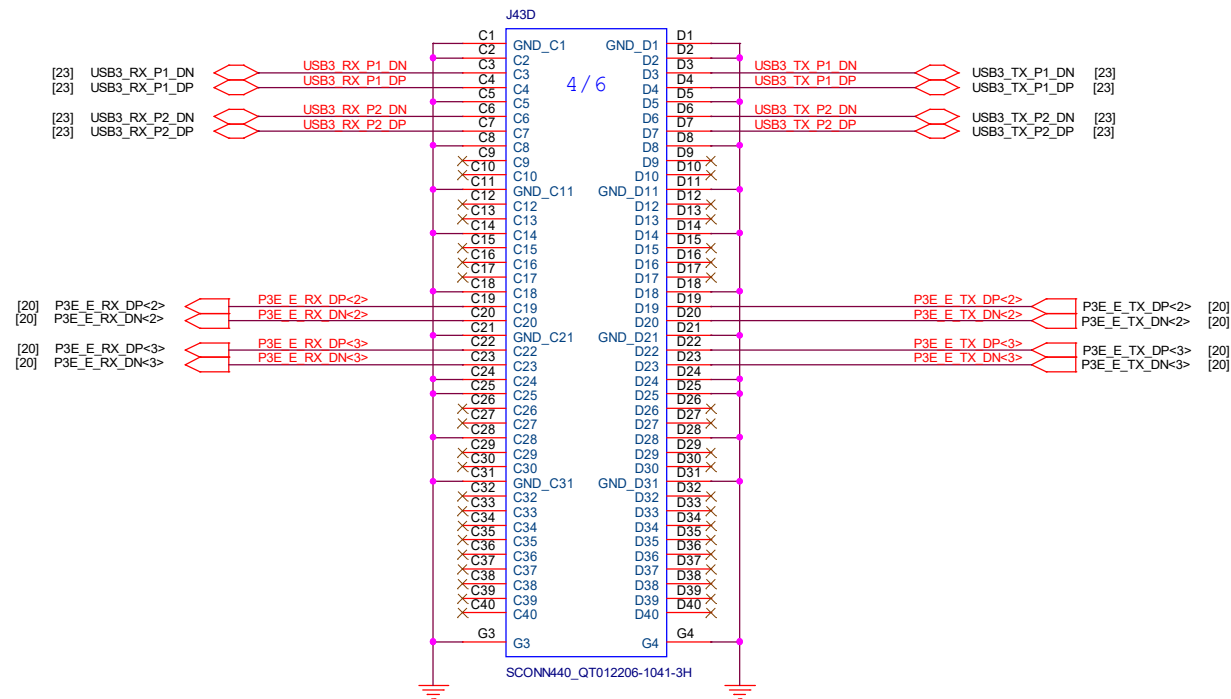
Date: Monday, November 26, 2018

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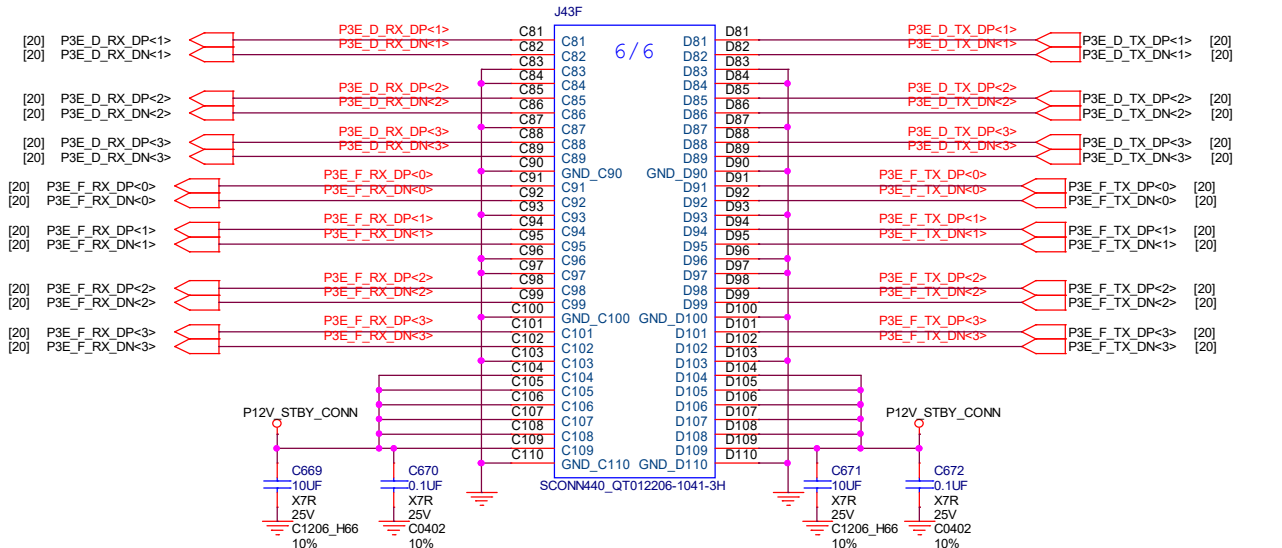
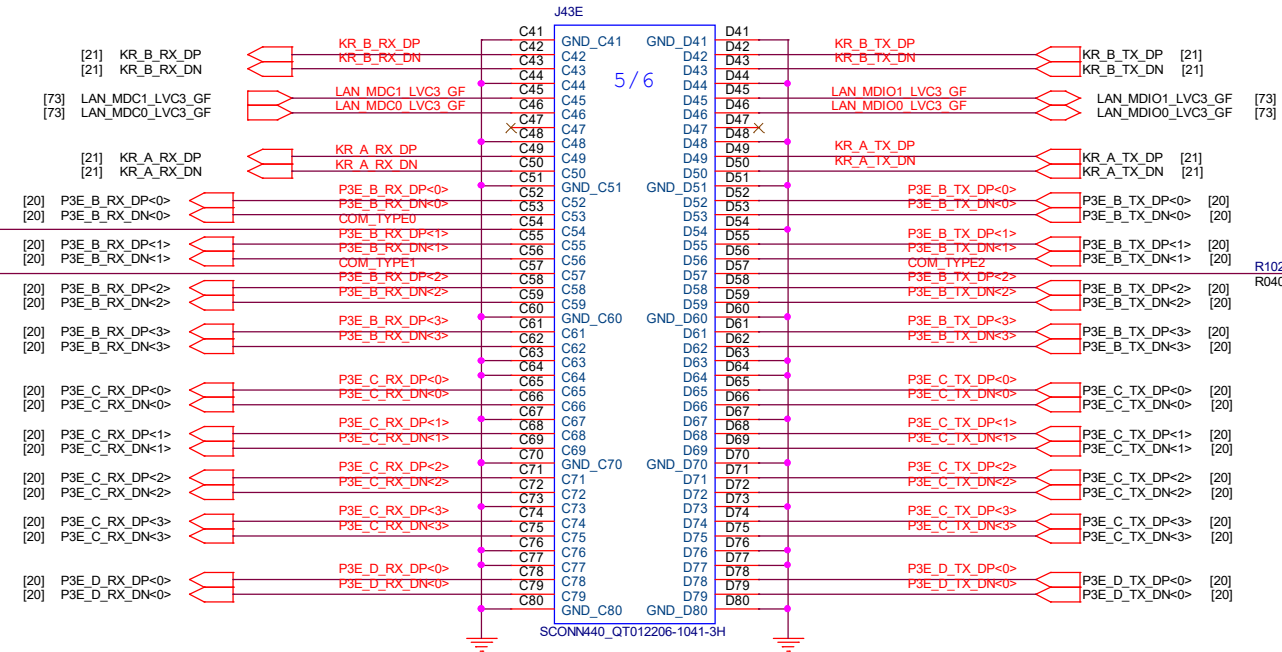
Rev 0.0

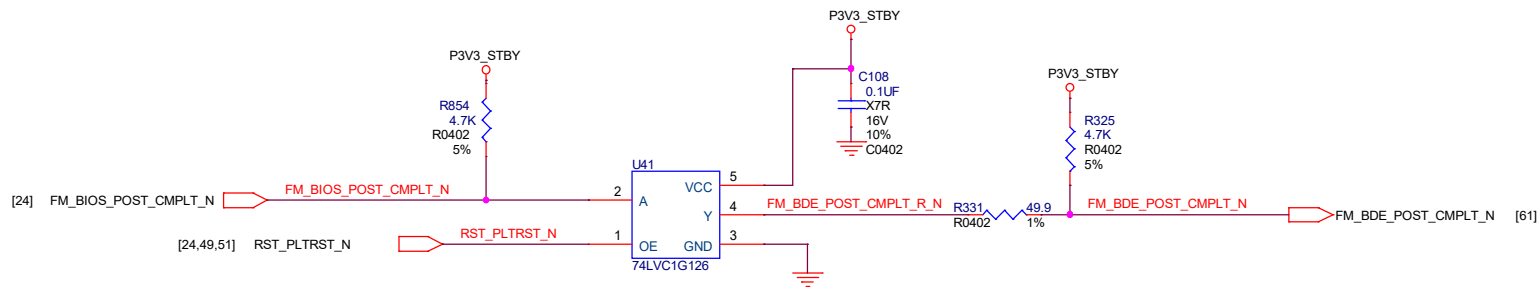
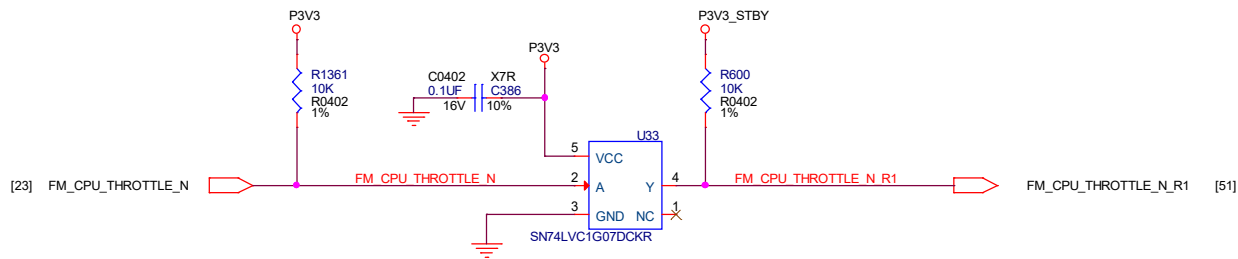
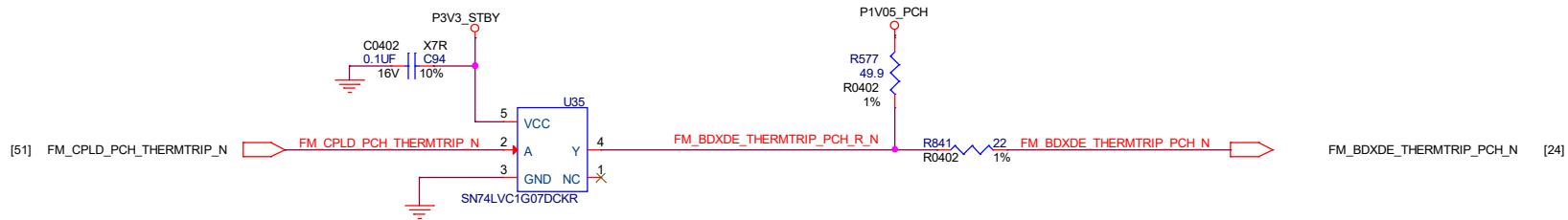
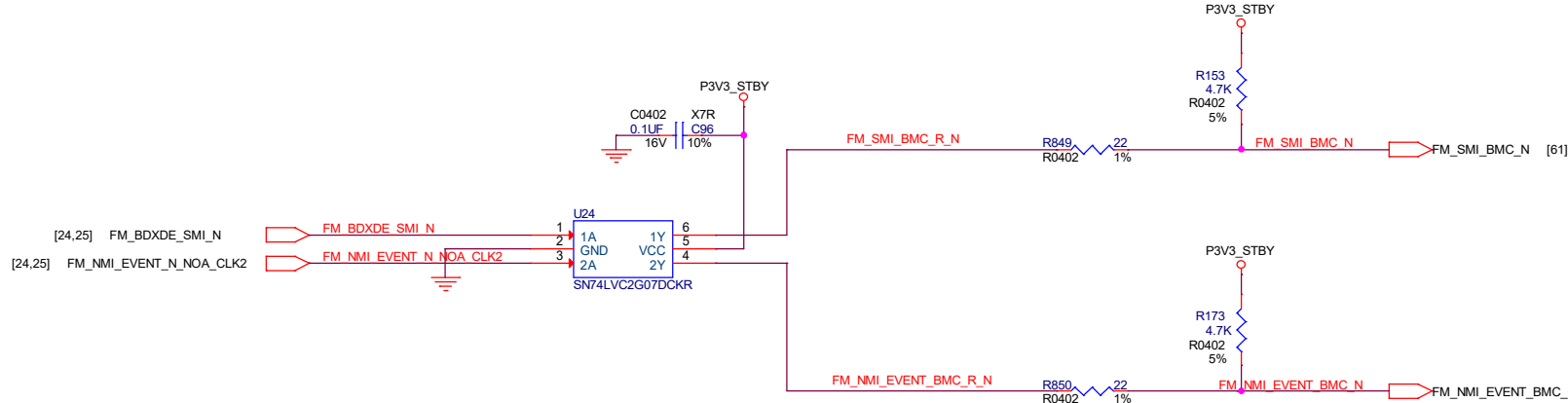


| TYPE10#                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | PDS |  | Dual use pin. Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier that a Rev 1.0 or a Rev 2.0/3.0 Module is installed. | All |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| TYPE10#                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |     |  |                                                                                                                                                                |     |
| NC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |     |  | Pin-out R2.0                                                                                                                                                   |     |
| PD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |     |  | Pin-out Type 10 pull down to ground with 47K resistor                                                                                                          |     |
| 12V                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |     |  | Pin-out R1.0                                                                                                                                                   |     |
| <p>This pin is reclaimed from the VCC_12V pool. In R1.0 Modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no connect for types 1-6. In R3.0 this pin is defined as a no connect for types 6 and 7. A Carrier can detect a R1.0 Module by the presence of 12V on this pin. R2.0 Module types 1-6 will no connect this pin. R3.0 Module types 6 and 7 will no connect this pin. Type 10 Modules <b>shall</b> pull this pin to ground through a 47K resistor.</p> |     |  |                                                                                                                                                                |     |

| TYPE2# | TYPE1# | TYPE0# |                                                 |
|--------|--------|--------|-------------------------------------------------|
| X      | X      | X      | Pin-out Type 10,<br>Pin-out Type 1 (deprecated) |
| NC     | NC     | NC     | Pin-out Type 2 (deprecated)                     |
| NC     | NC     | GND    | Pin-out Type 3 (deprecated)                     |
| NC     | GND    | NC     | Pin-out Type 4 (deprecated)                     |
| NC     | GND    | GND    | Pin-out Type 5 (deprecated)                     |
| GND    | NC     | NC     | Pin-out Type 6                                  |
| GND    | NC     | GND    | Pin-out Type 7                                  |

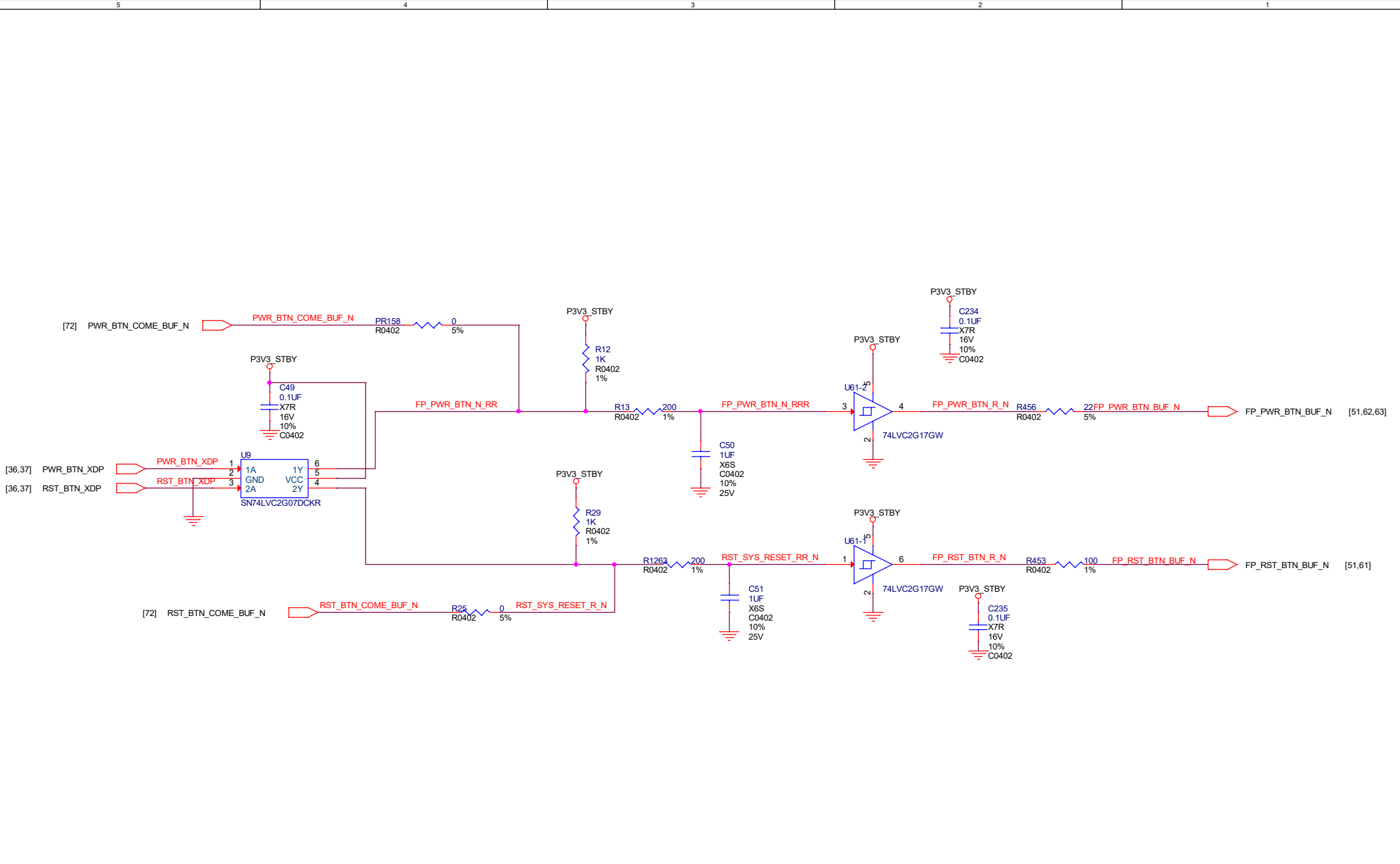
COM-E CONN CD 2





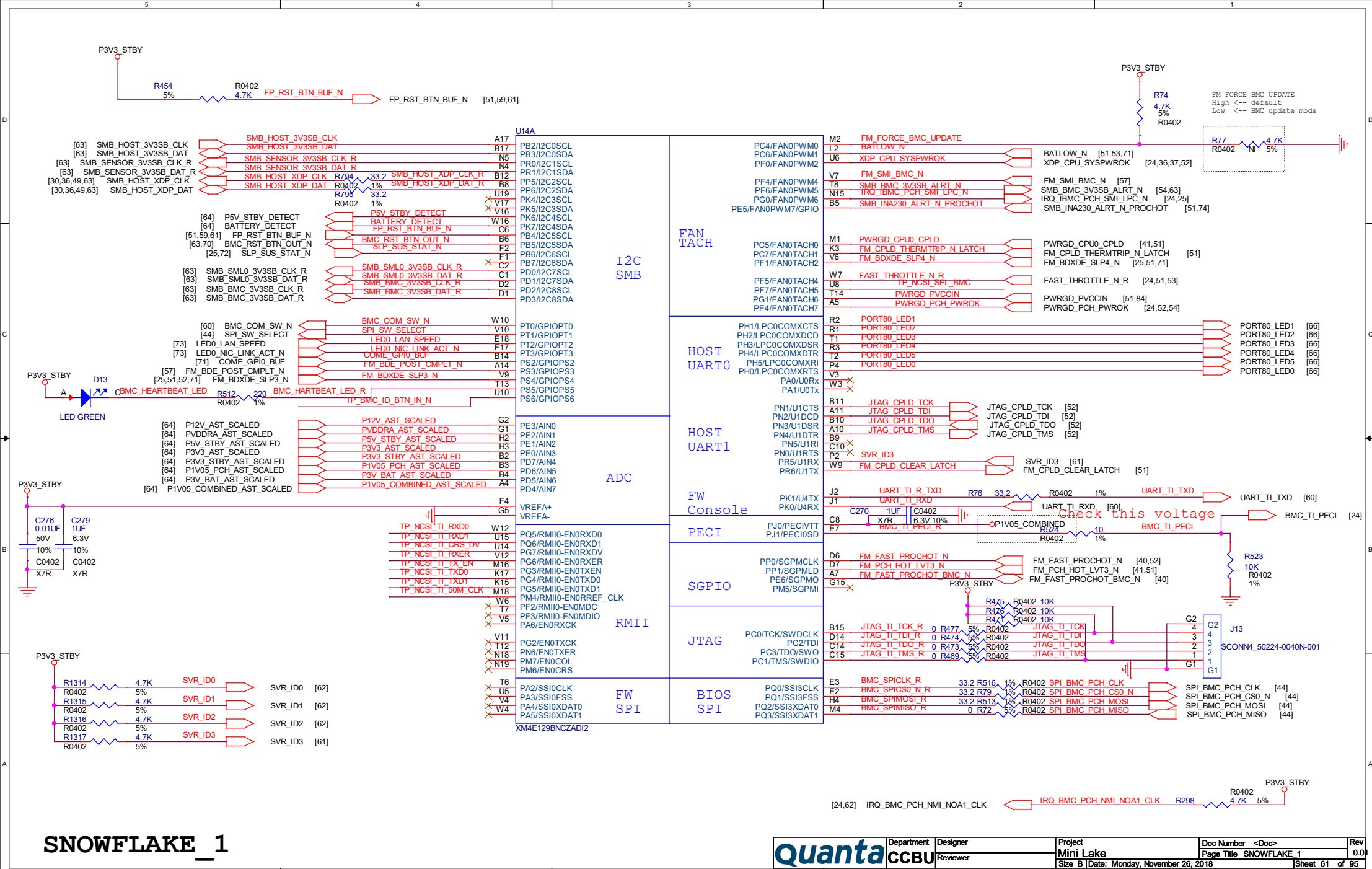
LEVEL\_SHIFT

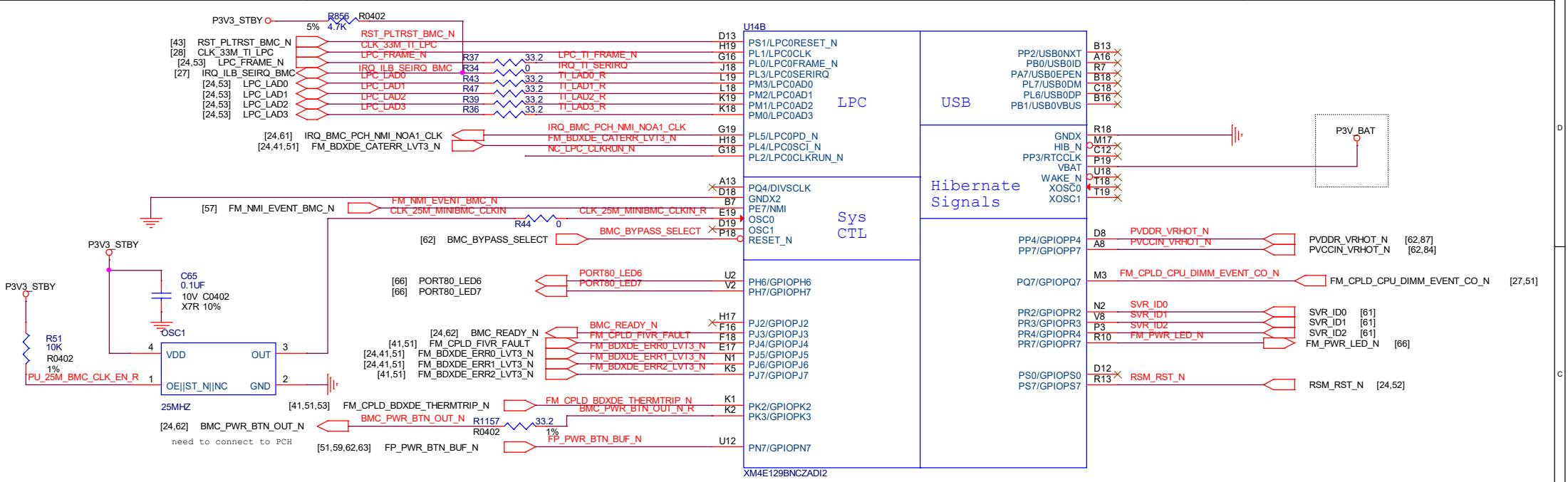




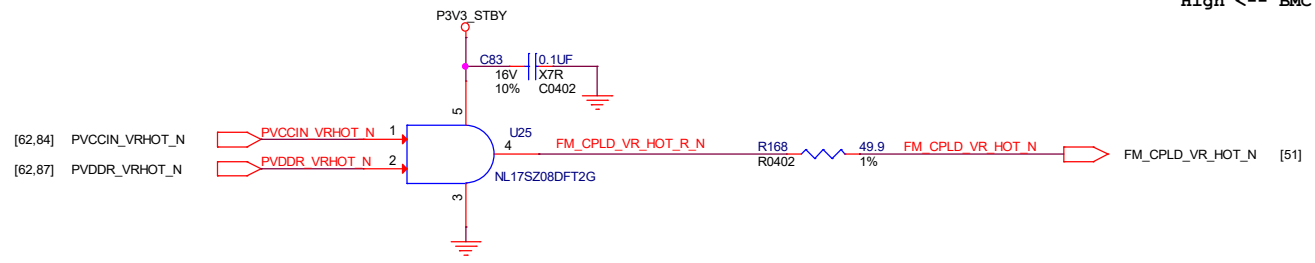
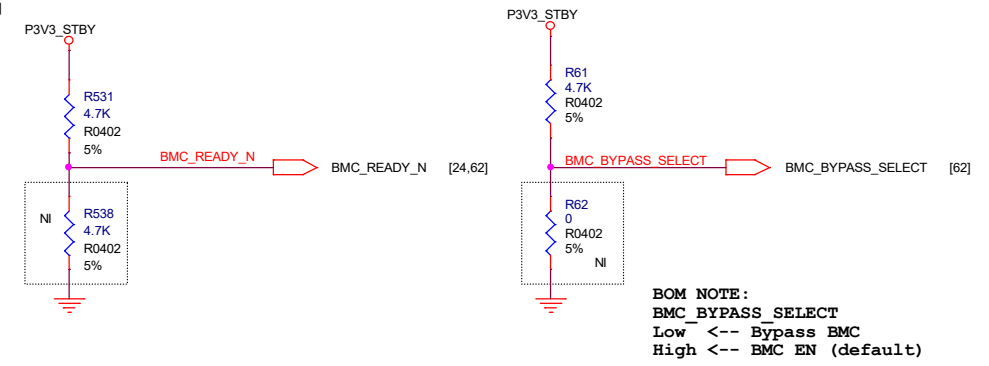
# PWR and SYS RESET Button



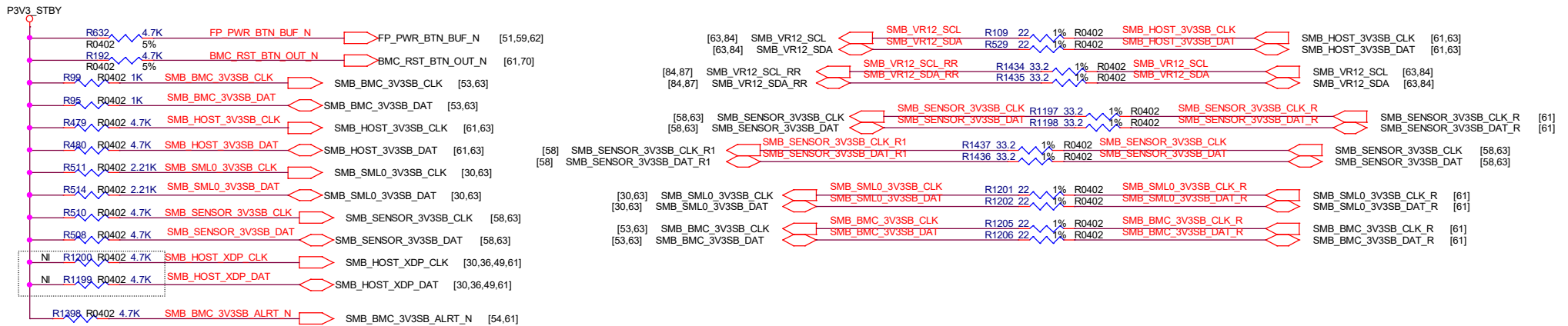
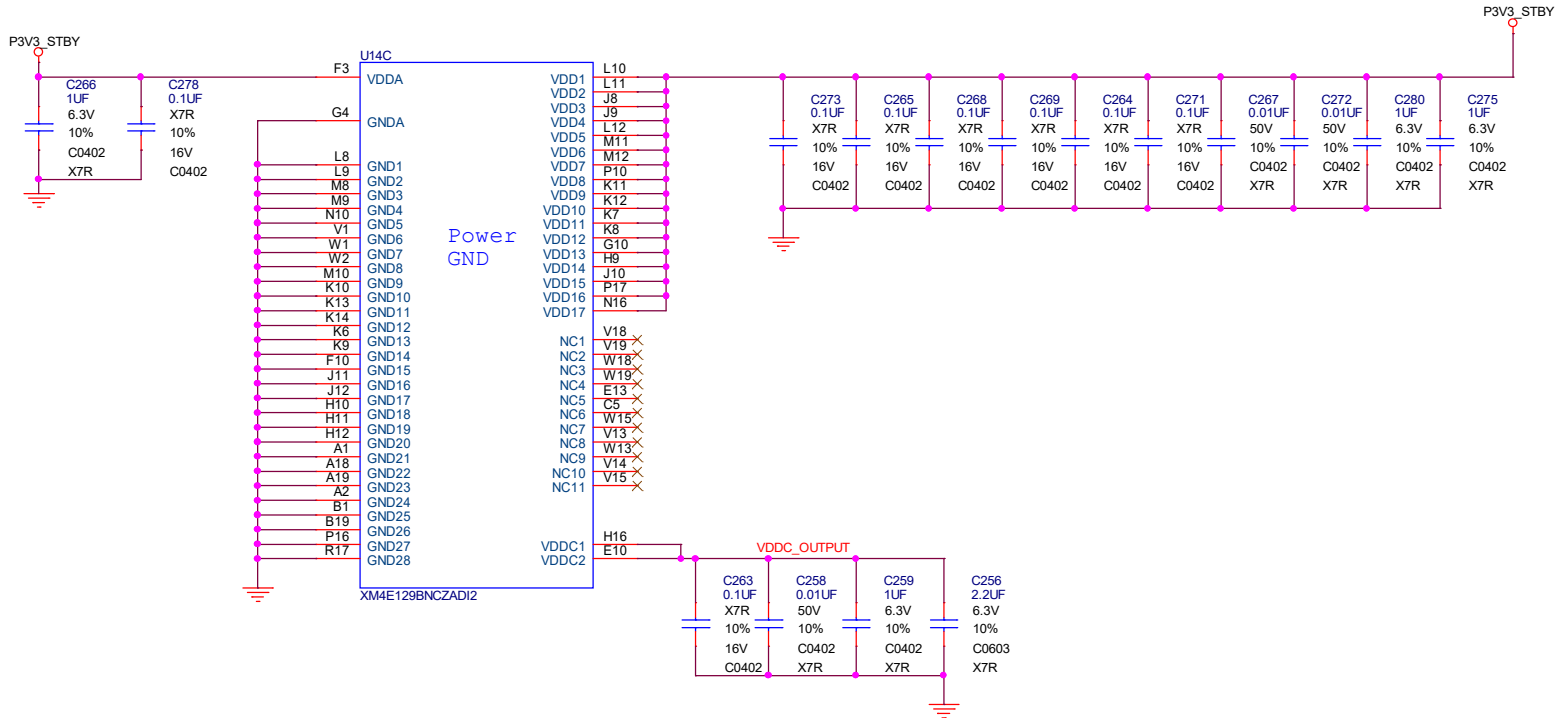




DESIGN NOTE : PWRBTN PASS THROUGH BRIDGE IC.



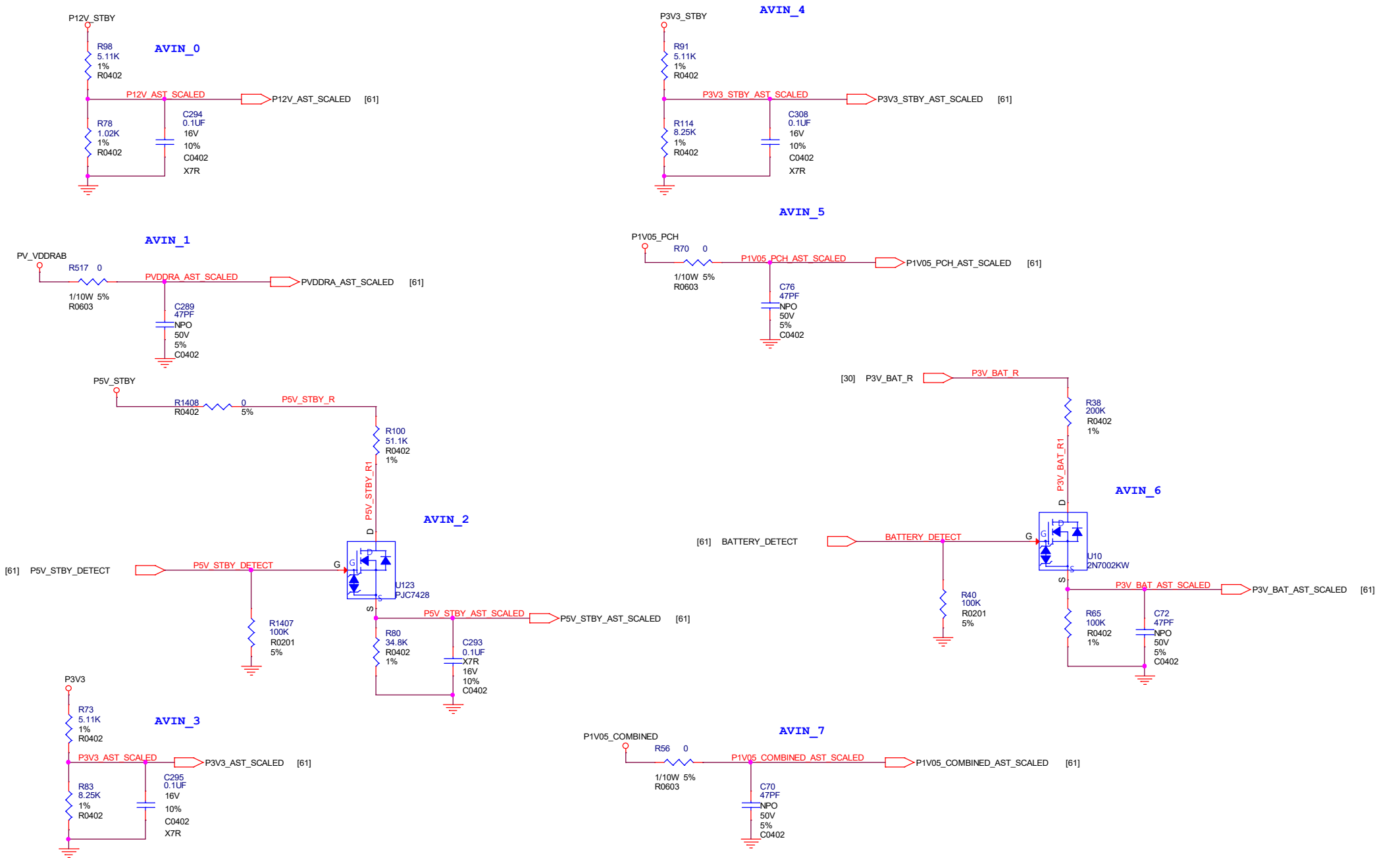
SNOWFLAKE\_2



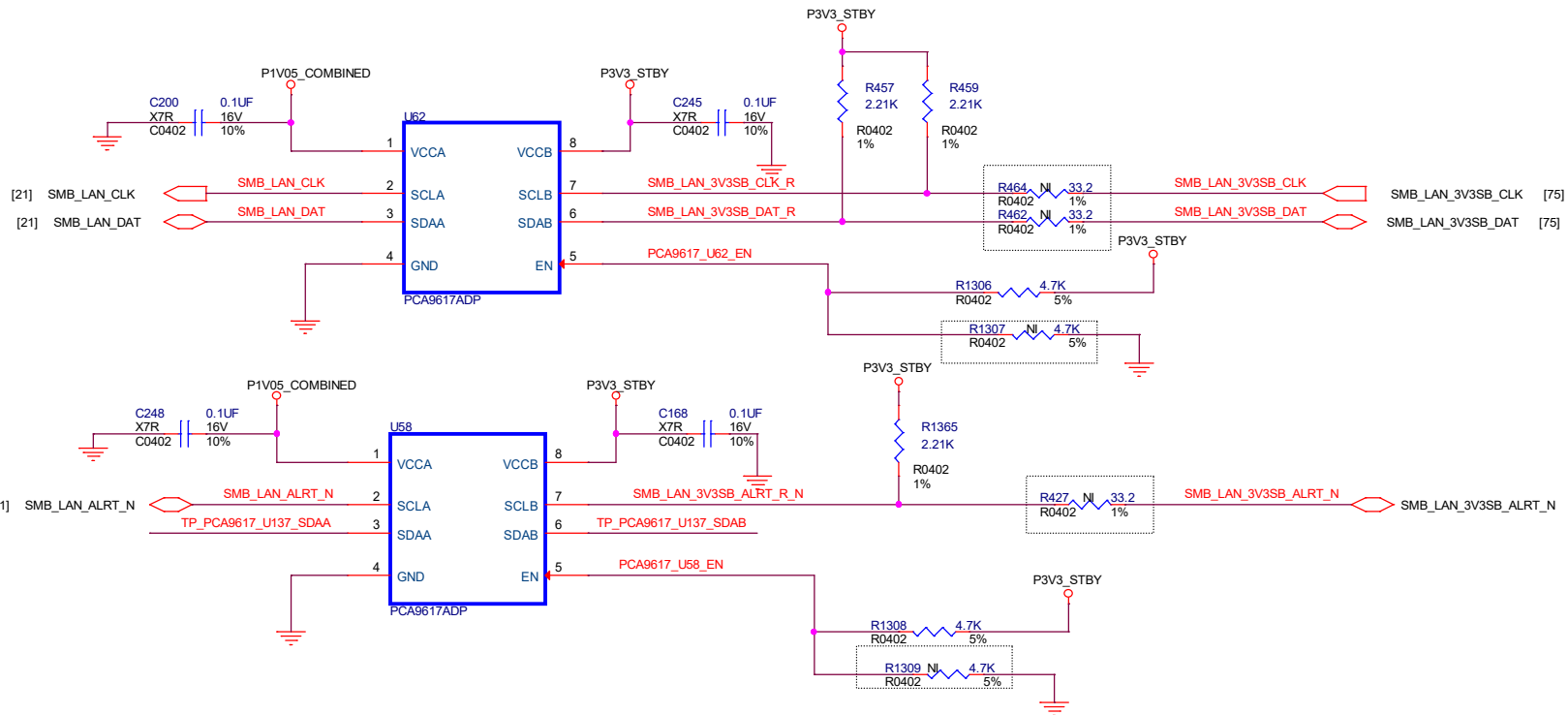
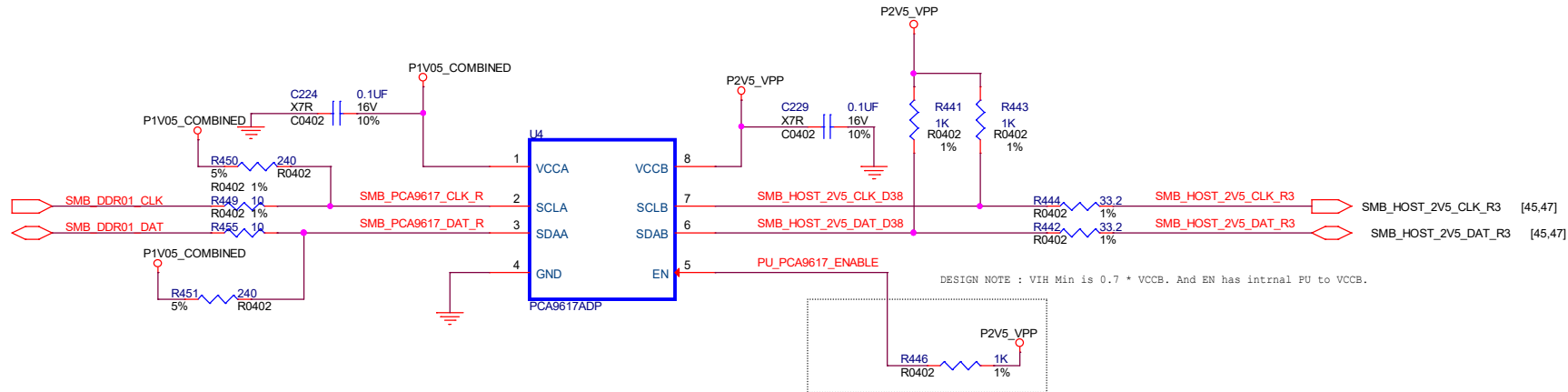
SNOWFLAKE\_3

|        |            |                                 |           |                                 |     |
|--------|------------|---------------------------------|-----------|---------------------------------|-----|
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# VOLTAGE MONITOR

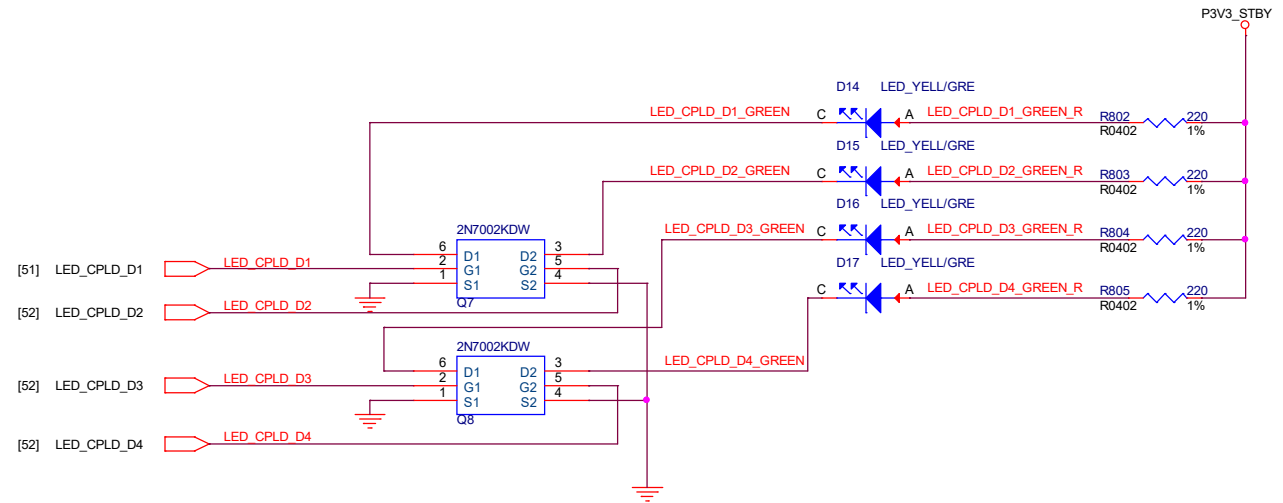
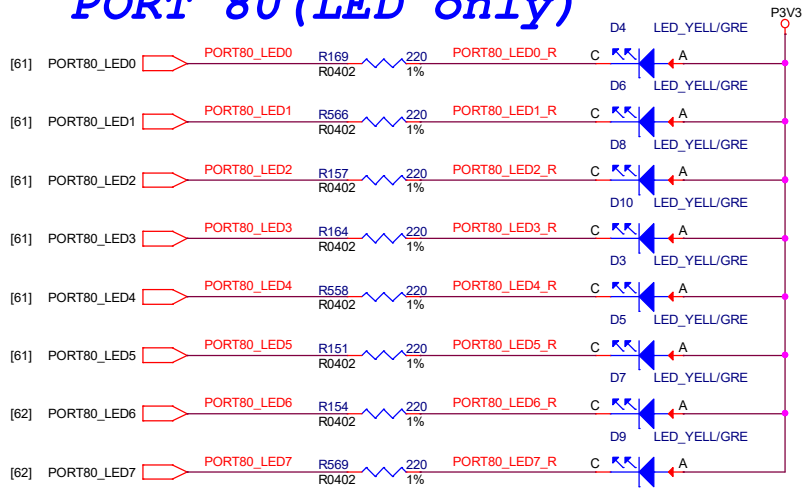


[30] SMB\_DDR01\_CLK  
[30] SMB\_DDR01\_DAT

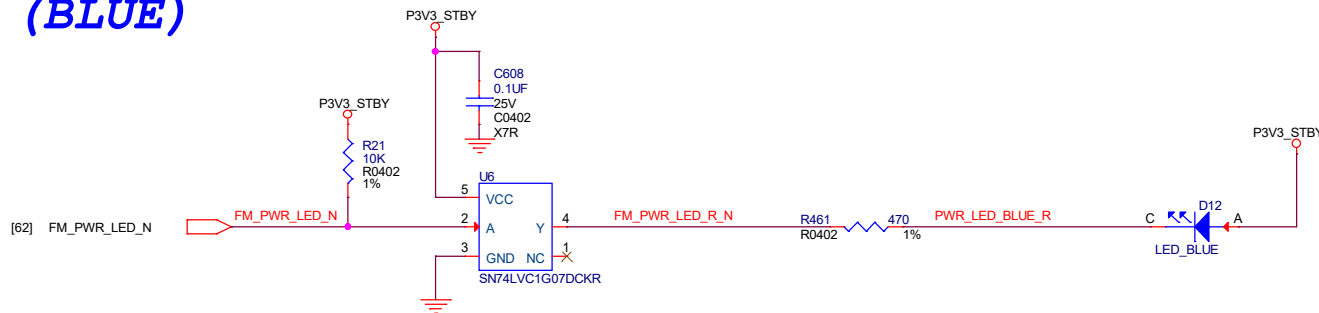


SMBUS ISOLATOR

## PORT 80 (LED only)

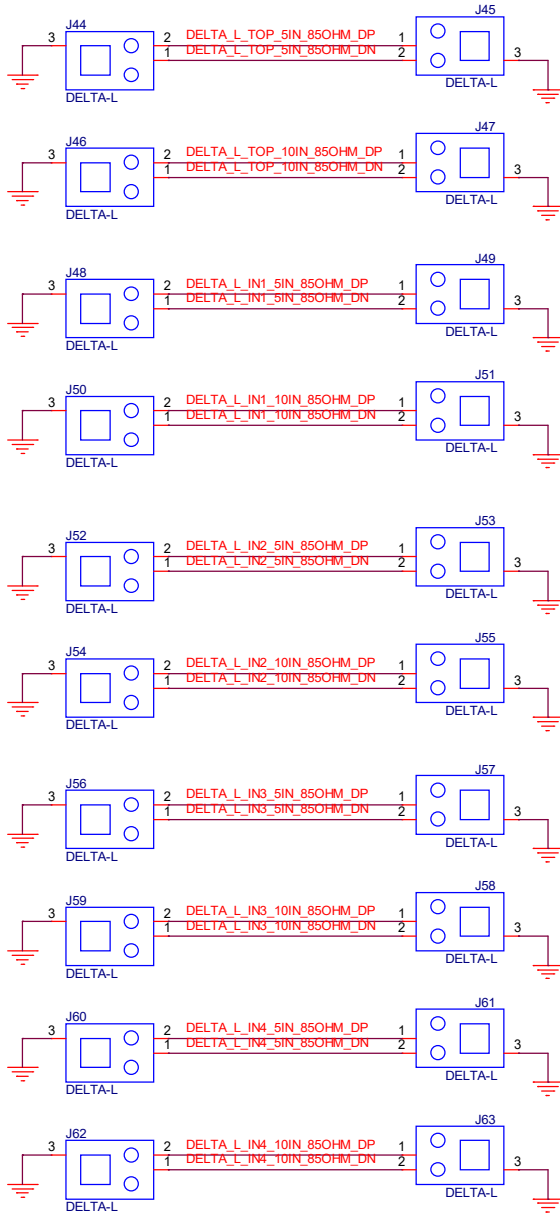


## POWER LED (BLUE)



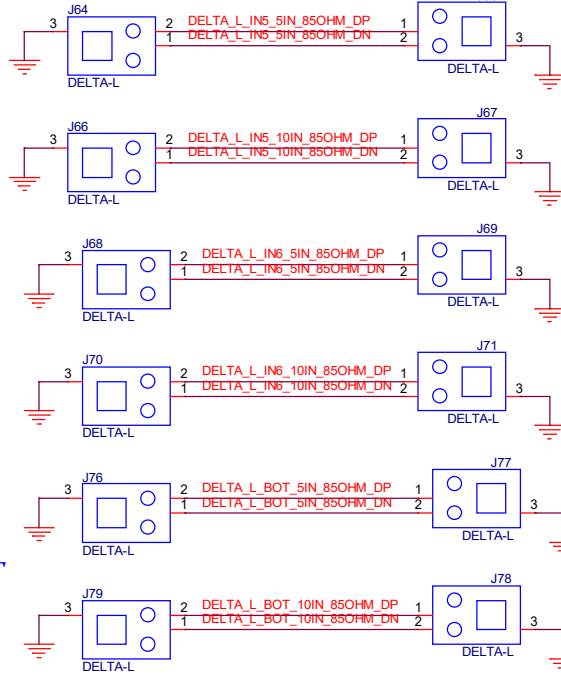
PWR/ PORT 80 LED

# DELTA-L



## DELTA-L AND TDR\_1

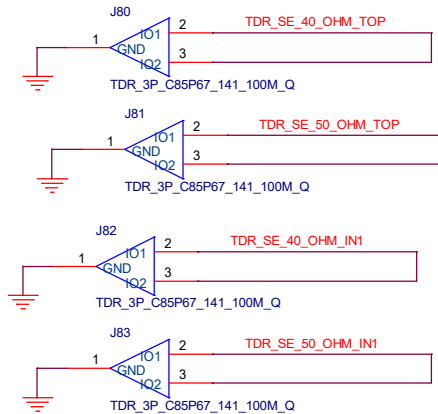
IN5



BOT

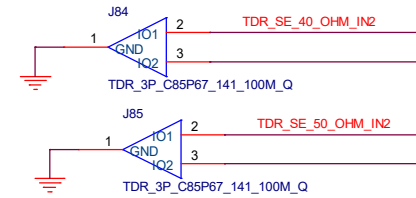
# TDR-SINGLE

TOP

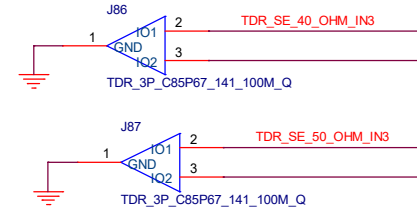


IN1

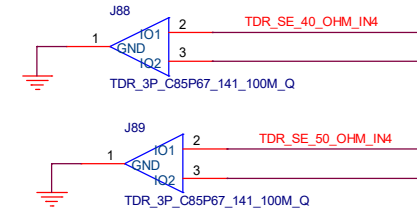
IN2



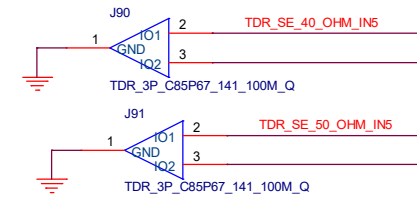
IN3



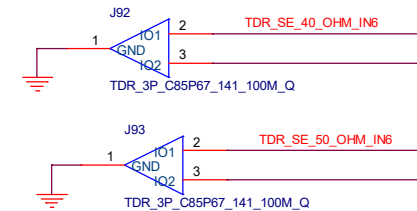
IN4



IN5

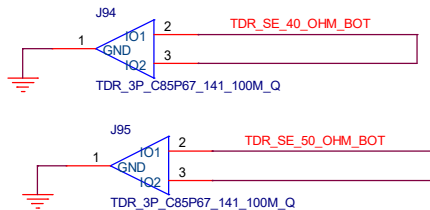


IN6



# TDR-SINGLE

BOT

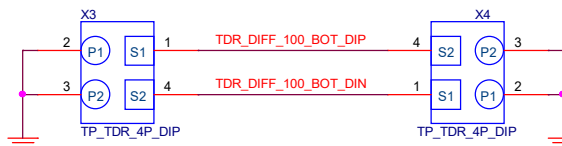


# TDR-DIFFERENTIAL

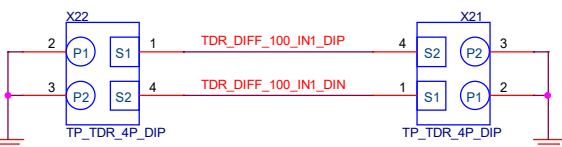
TOP



BOT



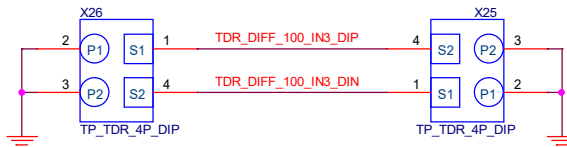
IN1



IN2



IN3



IN4



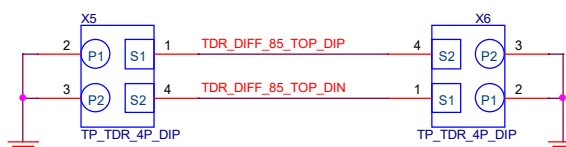
IN5



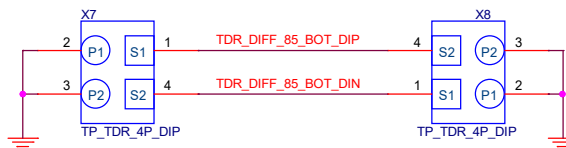
IN6



TOP



BOT



IN1



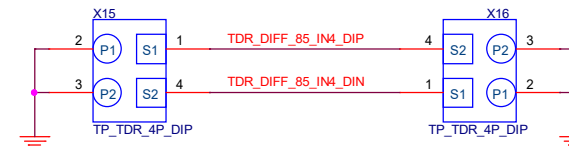
IN2



IN3



IN4



IN5

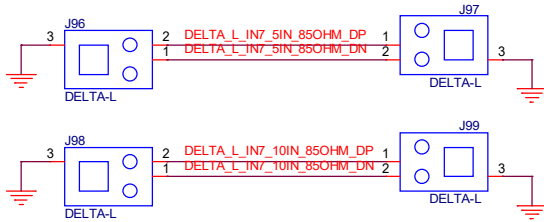


IN6

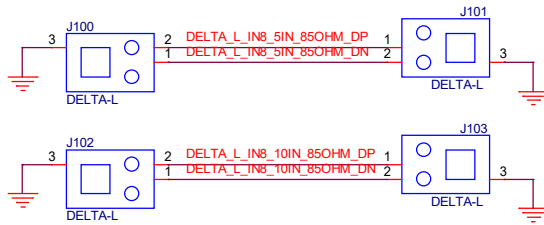


## DELTA-L

IN7

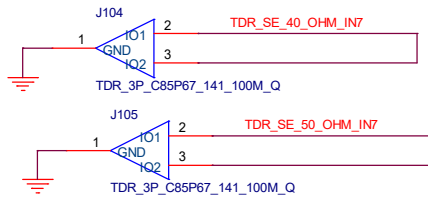


IN8

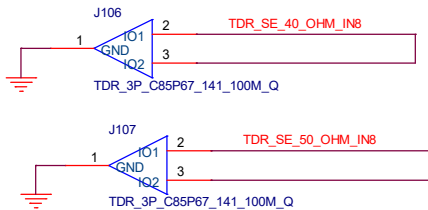


## TDR-SINGLE

IN7



IN8



## TDR-DIFFERENTIAL

IN7



IN8



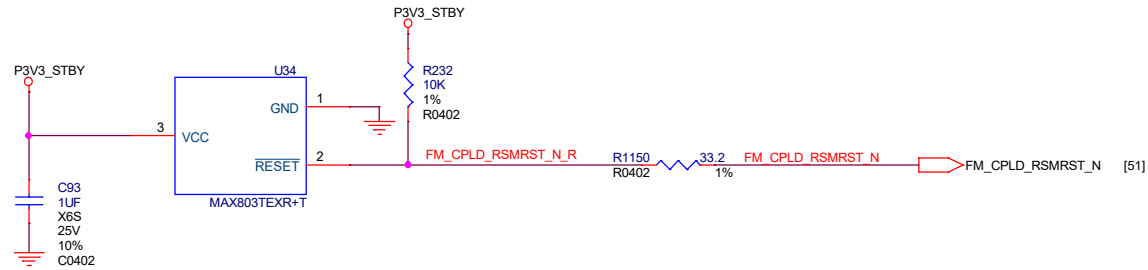
IN7



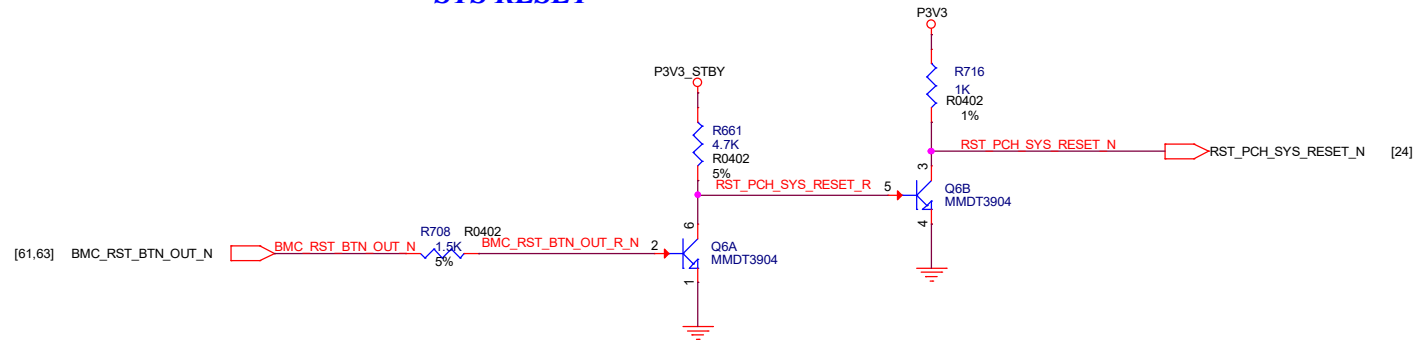
IN8



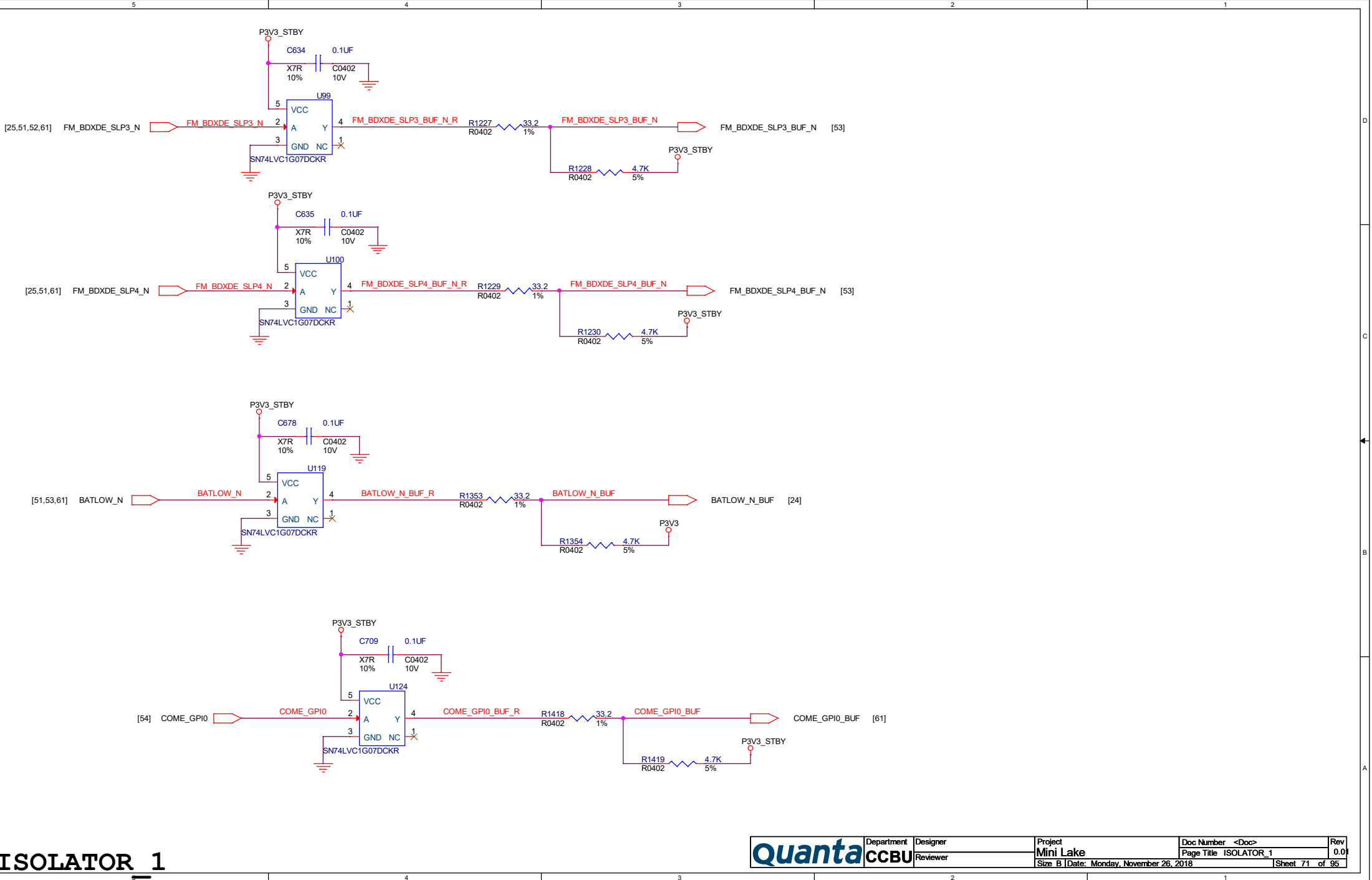
## RSMRST\_N



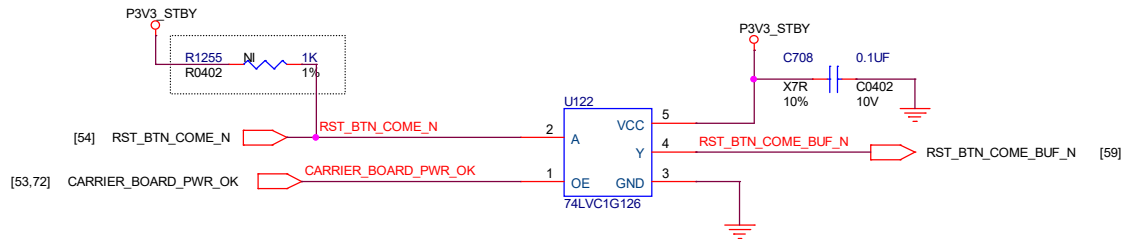
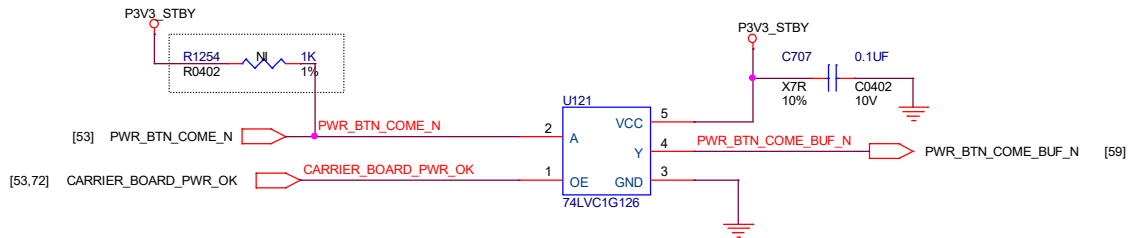
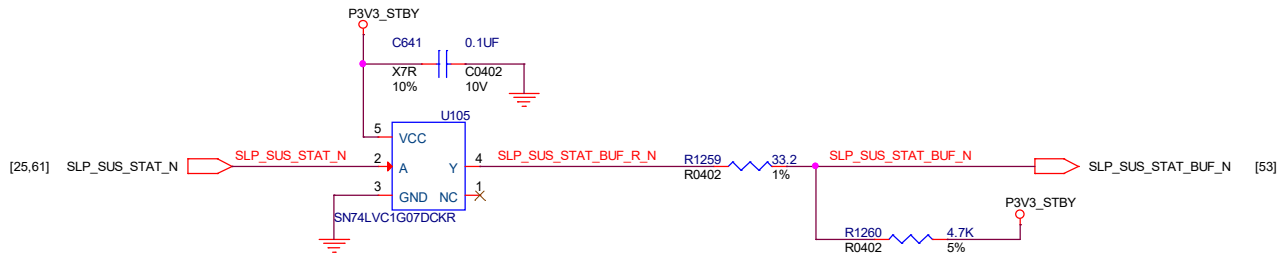
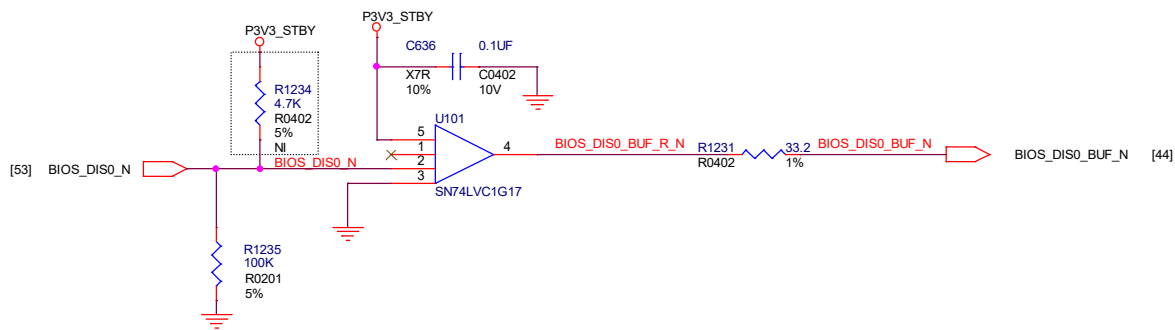
## SYS RESET



RSMRST

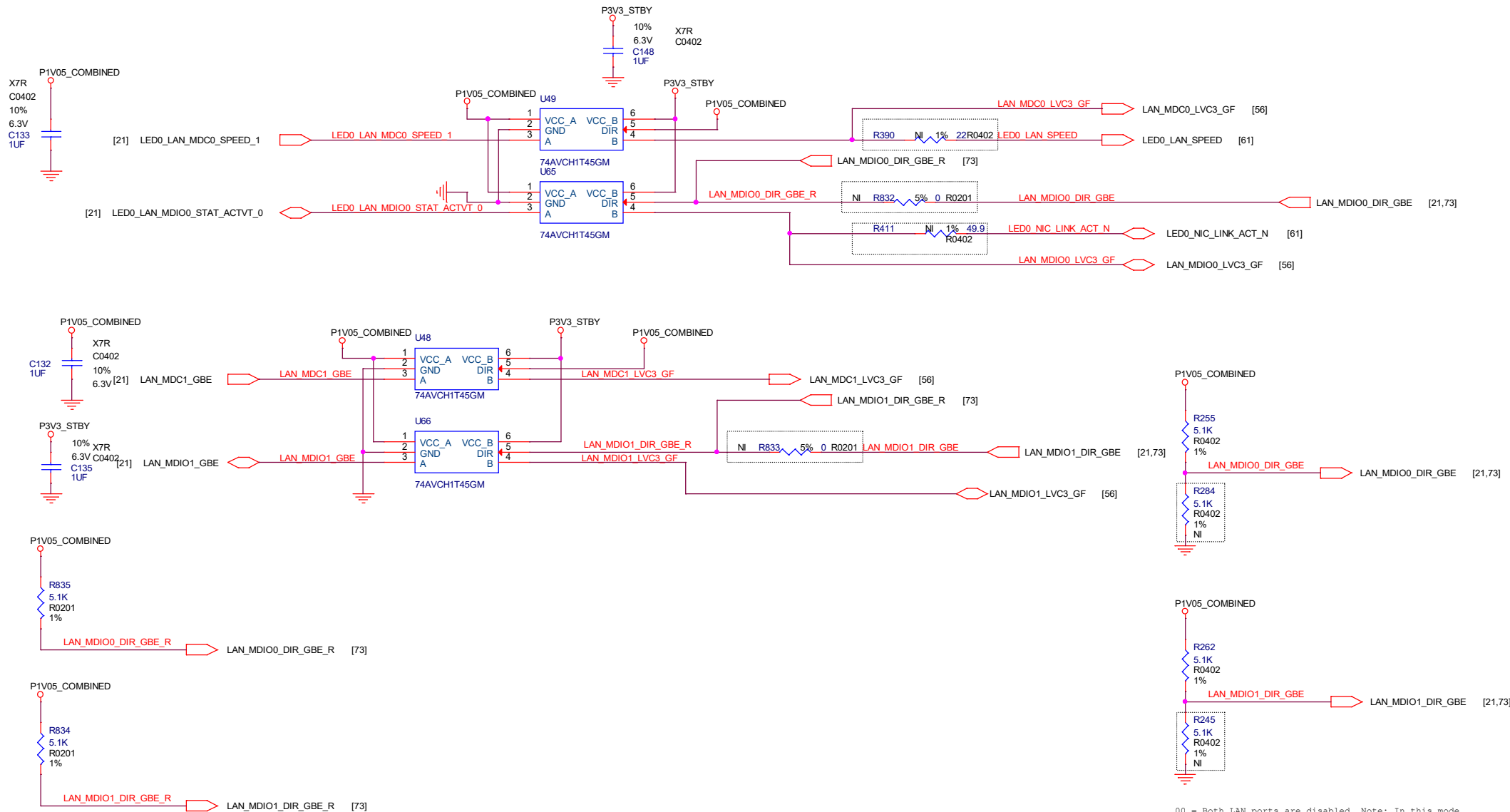


# ISOLATOR\_1



# ISOLATOR 2

|        |            |                                 |           |            |                |
|--------|------------|---------------------------------|-----------|------------|----------------|
| Quanta | Department | Designer                        | Project   | Doc Number | Rev            |
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|        |            | Date: Monday, November 26, 2018 |           |            |                |



# MDC/MDIO

Quanta

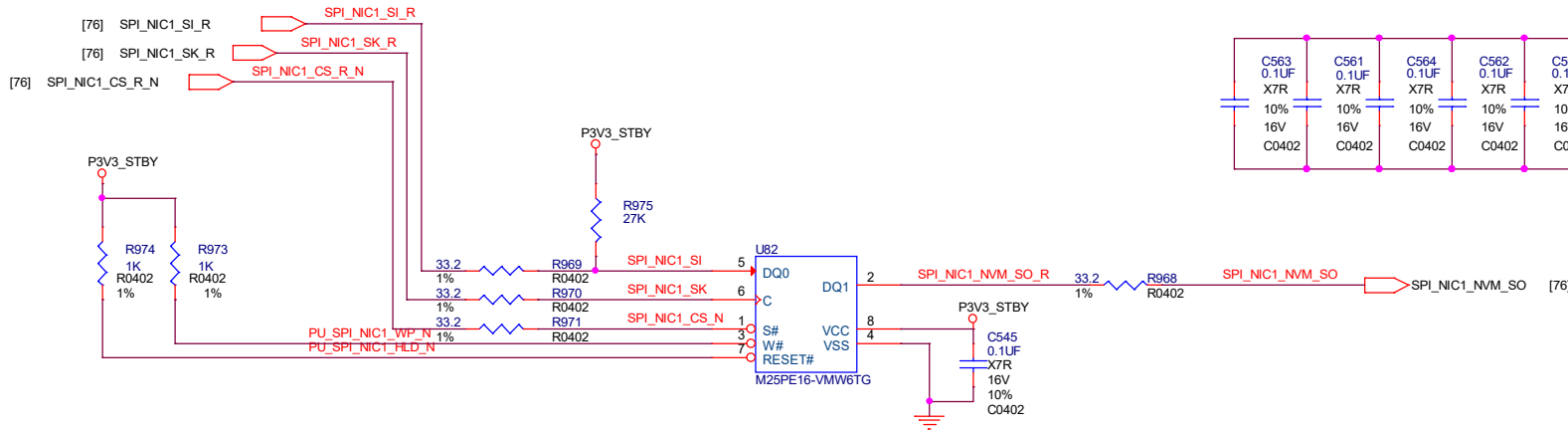
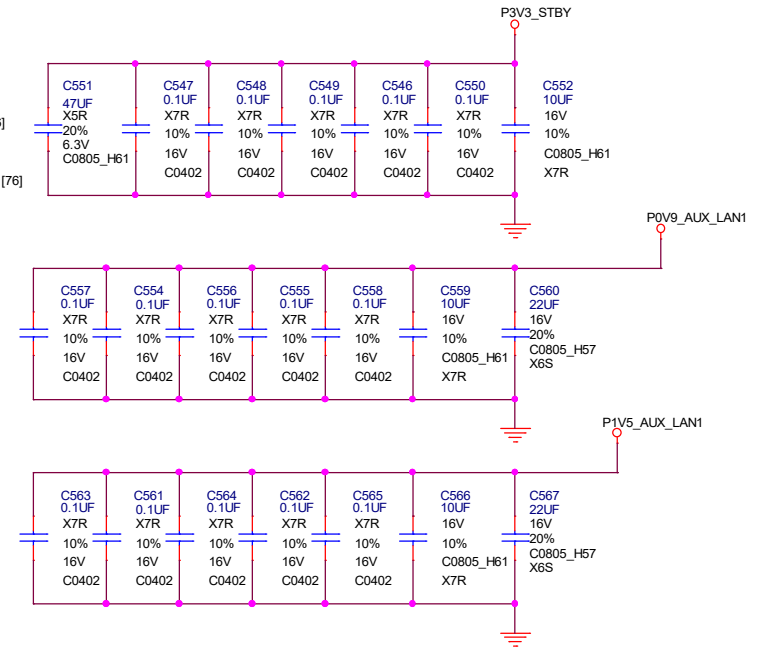
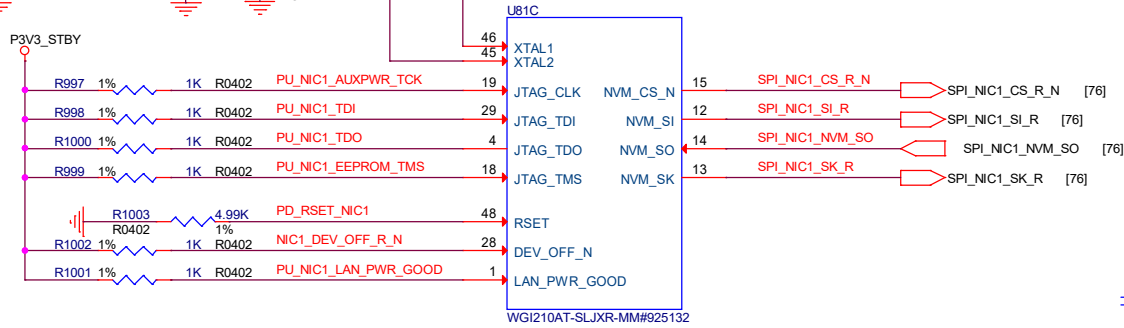
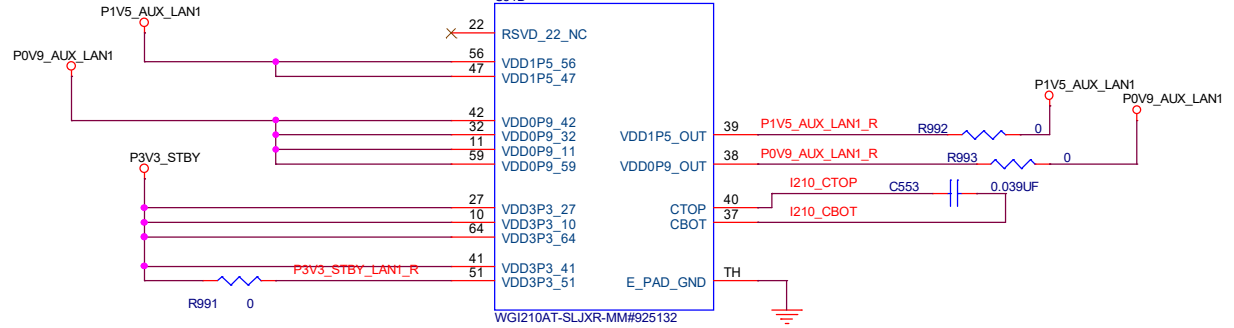
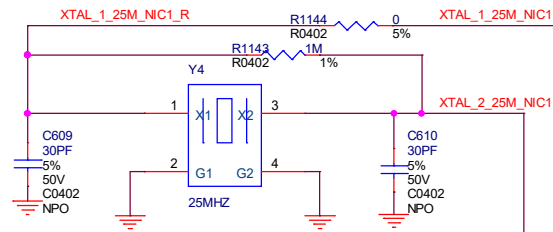
|            |          |                                          |                     |     |
|------------|----------|------------------------------------------|---------------------|-----|
| Department | Designer | Project                                  | Doc Number          | Rev |
| CCBU       |          | Mini Lake                                | <Doc>               | 0.0 |
| Reviewer   |          | Size B   Date: Monday, November 26, 2018 | Page Title MDC/MDIO |     |
|            |          |                                          | Sheet 73 of 95      |     |



LED0: ACTIVE  
LED1:SPD 100M  
LED2: SPD 1G

# I210 GbE PHY PCIE,MDI

|                                                                                       |            |                                 |                |                                           |     |
|---------------------------------------------------------------------------------------|------------|---------------------------------|----------------|-------------------------------------------|-----|
|  | Department | Designer                        | Project        | Doc Number                                | Rev |
|                                                                                       | CCBU       | Reviewer                        | Mini Lake      | <Doc><br>Page Title I210 GbE PHY PCIE,MDI | 0.0 |
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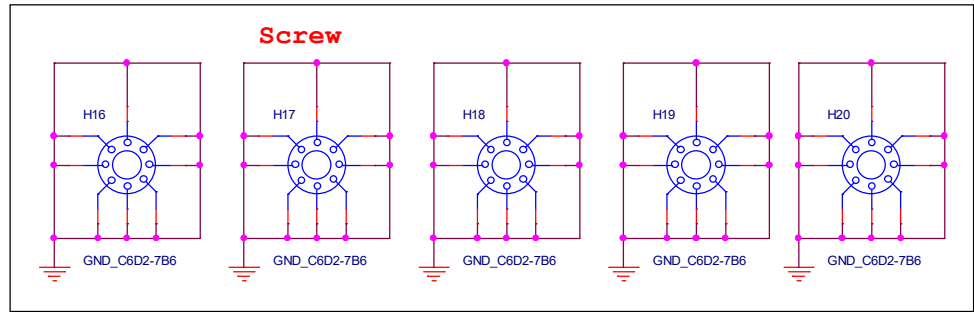


I210 GbE PHY JTAG, SPI, POWER

|  |            |          |           |            |                |
|--|------------|----------|-----------|------------|----------------|
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# Screw Hole

TP\_BIOS\_LABEL



**CE Logo**

DM1  
DUMMY\_SYMBOL  
CE\_LOGO\_5.8X5.08

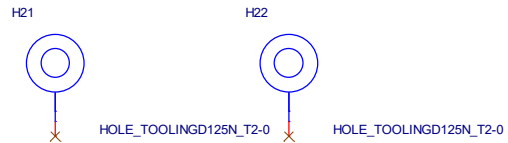
**WEEE**

DM2  
DUMMY\_SYMBOL  
WEEE

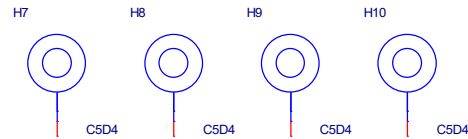
**Quanta LOGO**

DM3  
ME\_PART Symbol  
QUANTA\_LOGO\_2X7-6

## ICT Tooling Hole



## Heatsink HOLE



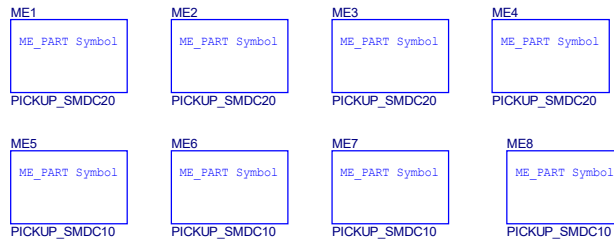
**PCB VENDOR LOGO**

DM5  
DUMMY\_SYMBOL  
PCB\_VENDOR\_LOGO\_15X8

**PCB FREE**

DM7  
DUMMY\_SYMBOL  
PB-E1\_SMALL

## Suction nozzle



**SCREW**

Blank drawing area with grid lines and dimensions.

Grid lines are labeled A, B, C, D vertically and 1, 2, 3, 4, 5 horizontally.

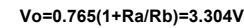
Dimensions are indicated by arrows and text:

- Vertical dimension: 10' 0" (from A to D)
- Horizontal dimension: 10' 0" (from 1 to 5)

BLANK

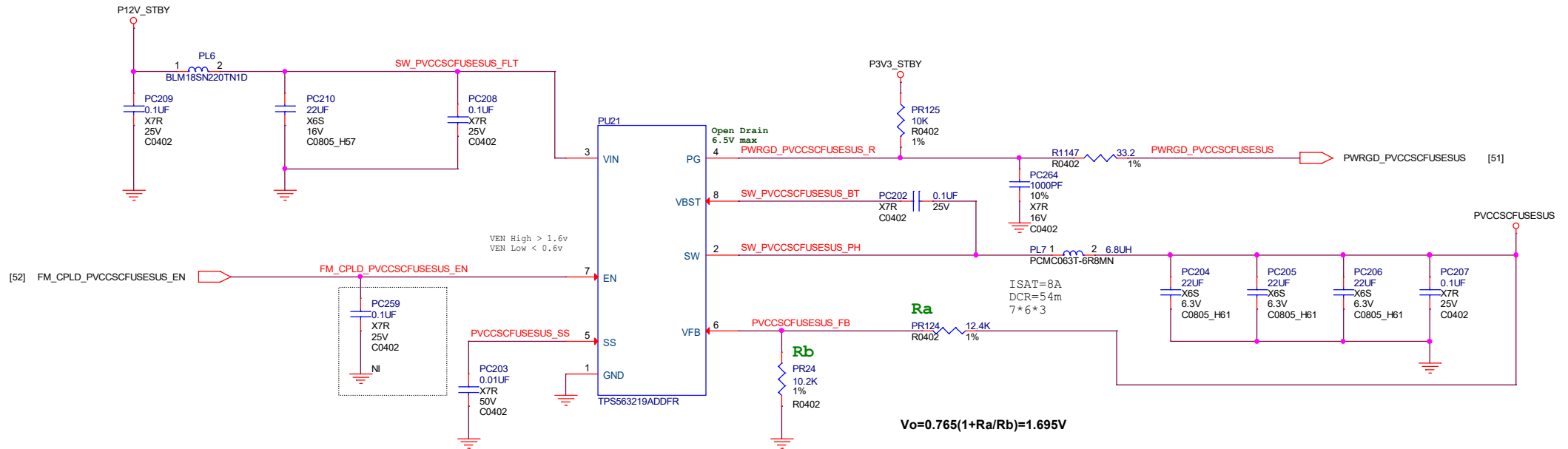
|               |            |          |                                 |            |                |
|---------------|------------|----------|---------------------------------|------------|----------------|
| <b>Quanta</b> | Department | Designer | Project                         | Doc Number | Rev            |
|               | CCBU       | Reviewer | Mini Lake                       | <Doc>      | 0.0            |
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Follow grangeville\_pdg\_2\_2 p355



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Design specification  
PVCCSCFUSESUS  
Output Voltage =  $1.7V \pm 2\%$   
Output Ripple & Noise  $\pm 10mV$   
Transient Tolerance =  $\pm 5\%$   
TDC = 1.3A  
Max current = 2A  
Over-Current Protection(IC Rating) = 4.2A  
Current Step = 1.0A  
Slew Rate = 0.5A/us  
Work Frequency = 650kHz  
Efficiency > 85% @TDC  
Follow grangeville\_pdg\_2\_2 p353



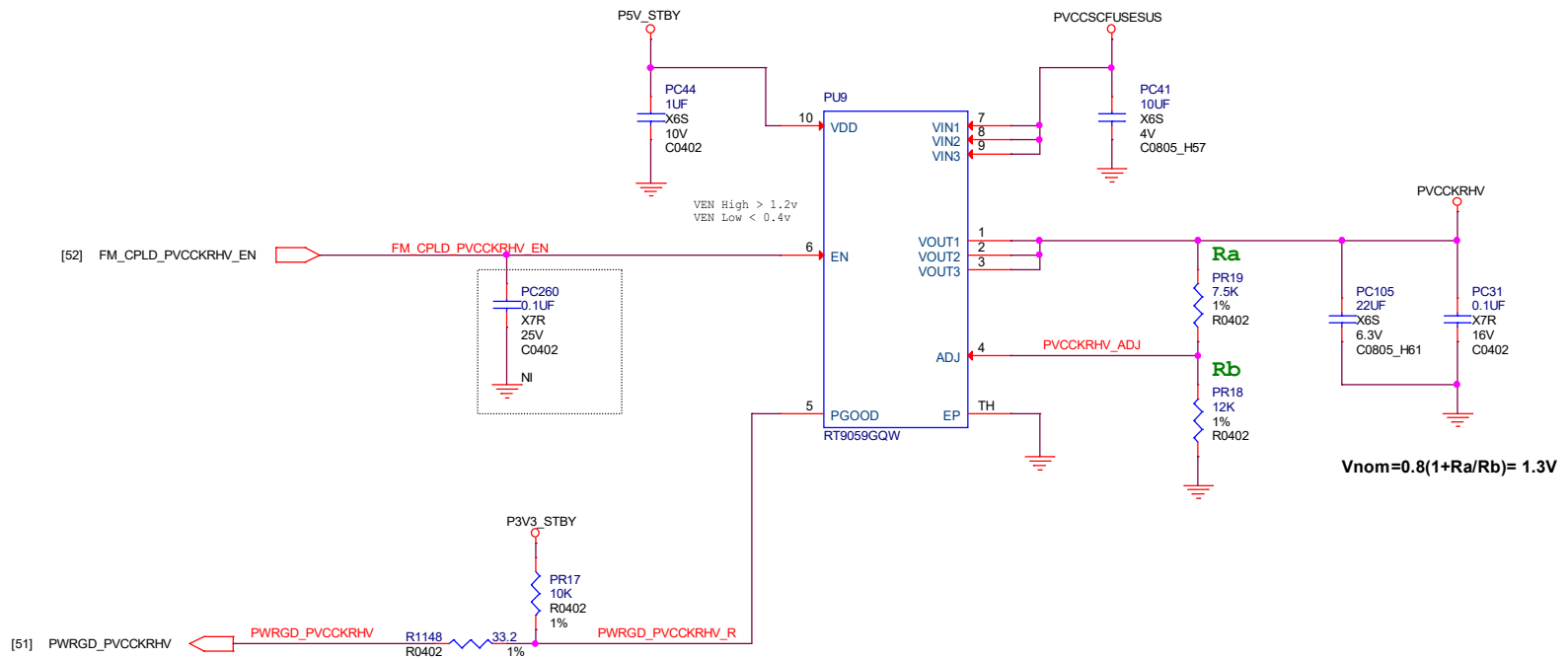
$$V_o = 0.765(1 + R_a/R_b) = 1.695V$$

**PVCCSCFUSESUS**

P2V5\_VPP



Design specification  
PVCCRHV  
Output Voltage = 1.3V±2.1%  
Output Ripple & Noise ±4mV  
Transient Tolerance = ±4.0%  
TDC = 0.25A  
Max current = 0.5A  
Current Step = 0.15A  
Slew Rate = 11A/us  
PD=(1.7V-1.3V)\*0.25A=0.1W  
Follow grangeville\_pdg\_2\_2 p356

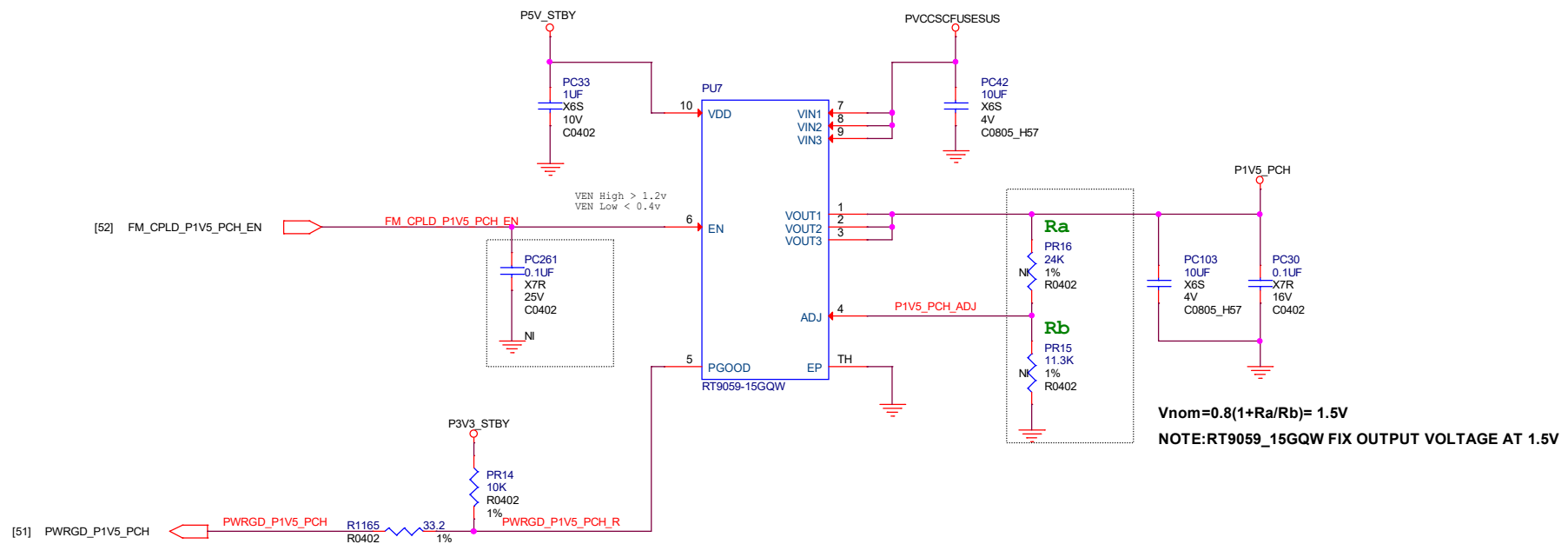


PVCCRHV

Quanta

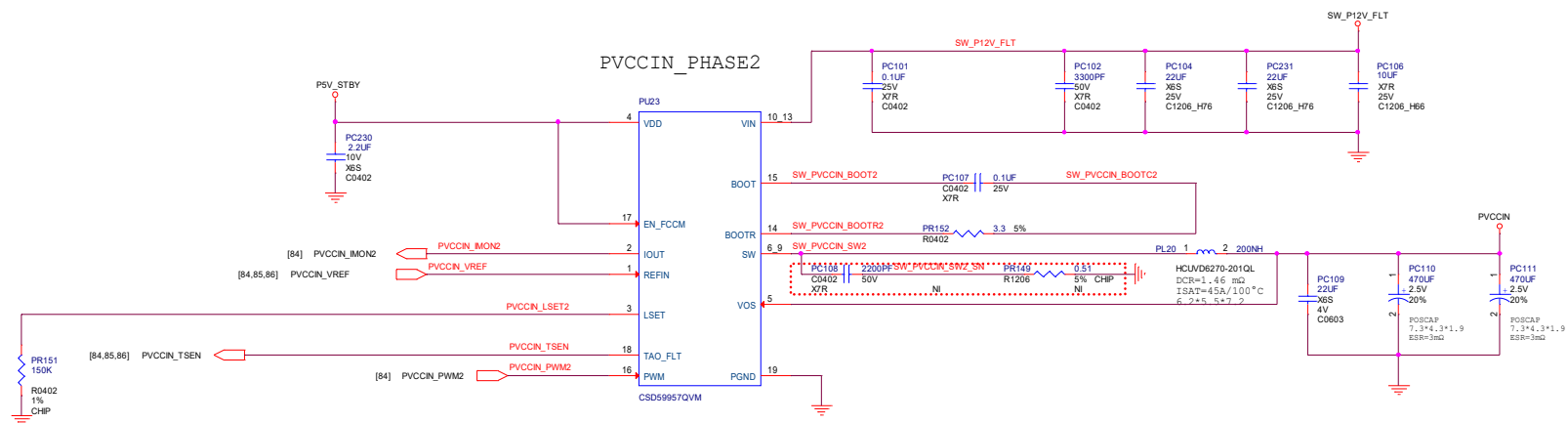
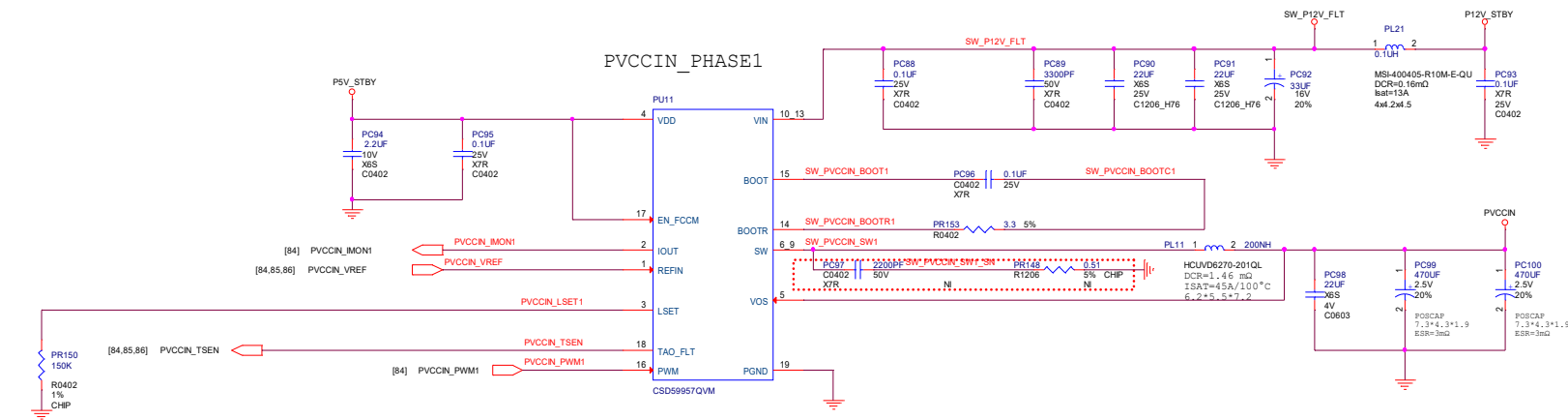
|            |          |                                          |                    |                |
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| Department | Designer | Project                                  | Doc Number         | Rev            |
| CCBU       | Reviewer | Mini Lake                                | <Doc>              | 0.0            |
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Design specification  
P1V5\_PCH  
Output Voltage = 1.5V±3%  
Output Ripple & Noise ±1%  
Transient Tolerance = ±5.0%  
TDC = 0.2A  
Max current = 0.3A  
Current Step = 0.03A  
Slew Rate = 1A/us  
PD=(1.7V-1.5V)\*0.2A=0.04W  
Follow grangeville\_pdg\_2\_2 p358

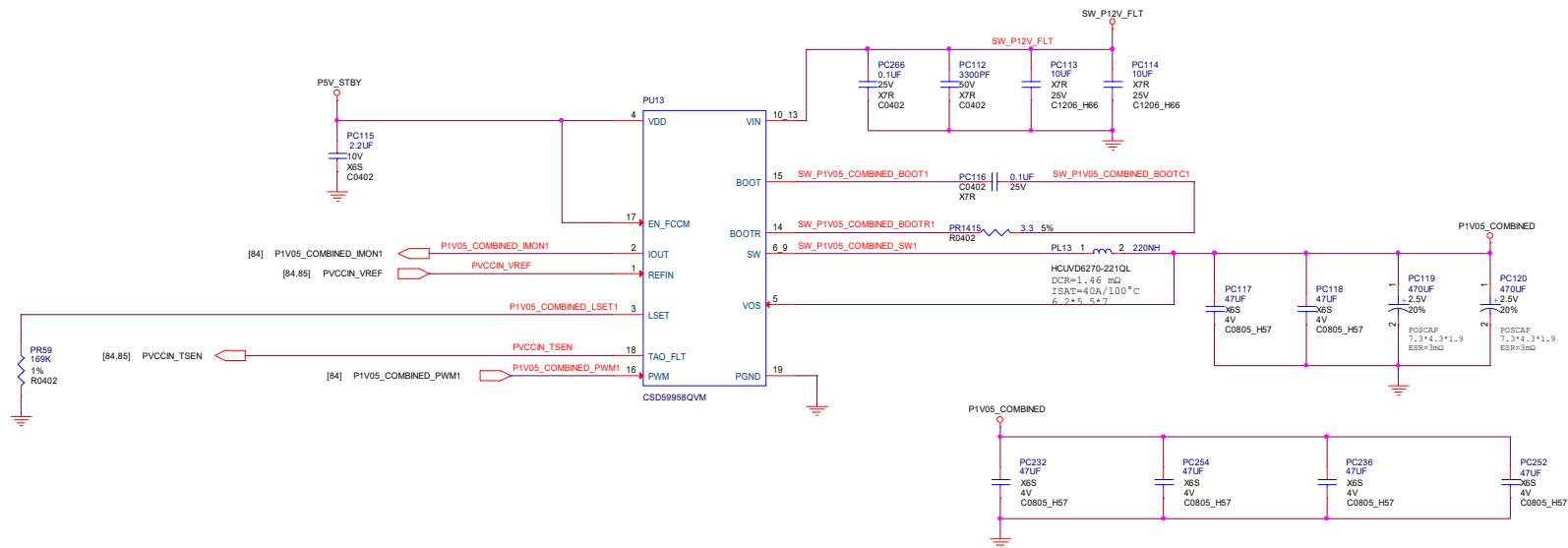


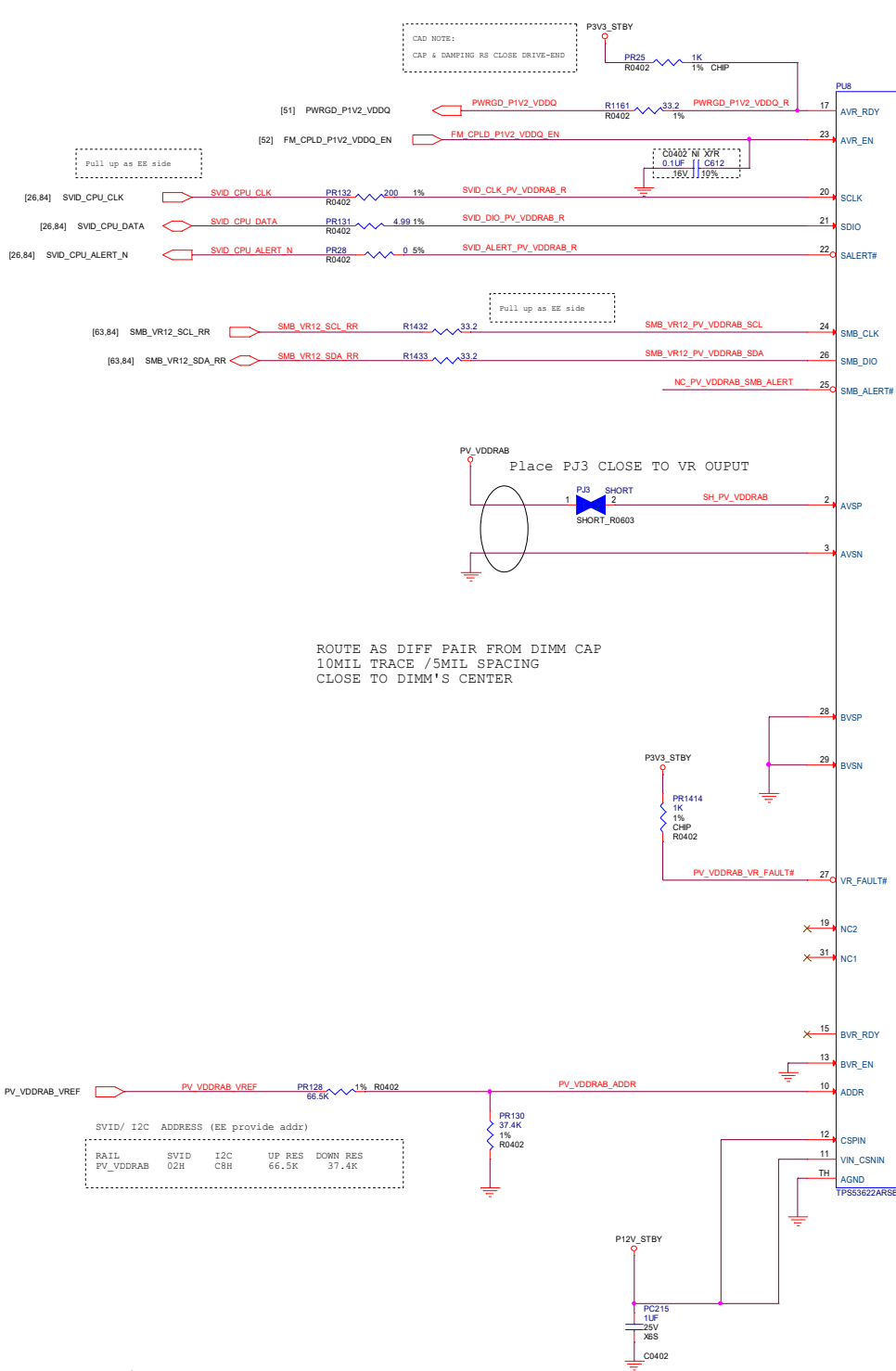
**P1V5 PCH**





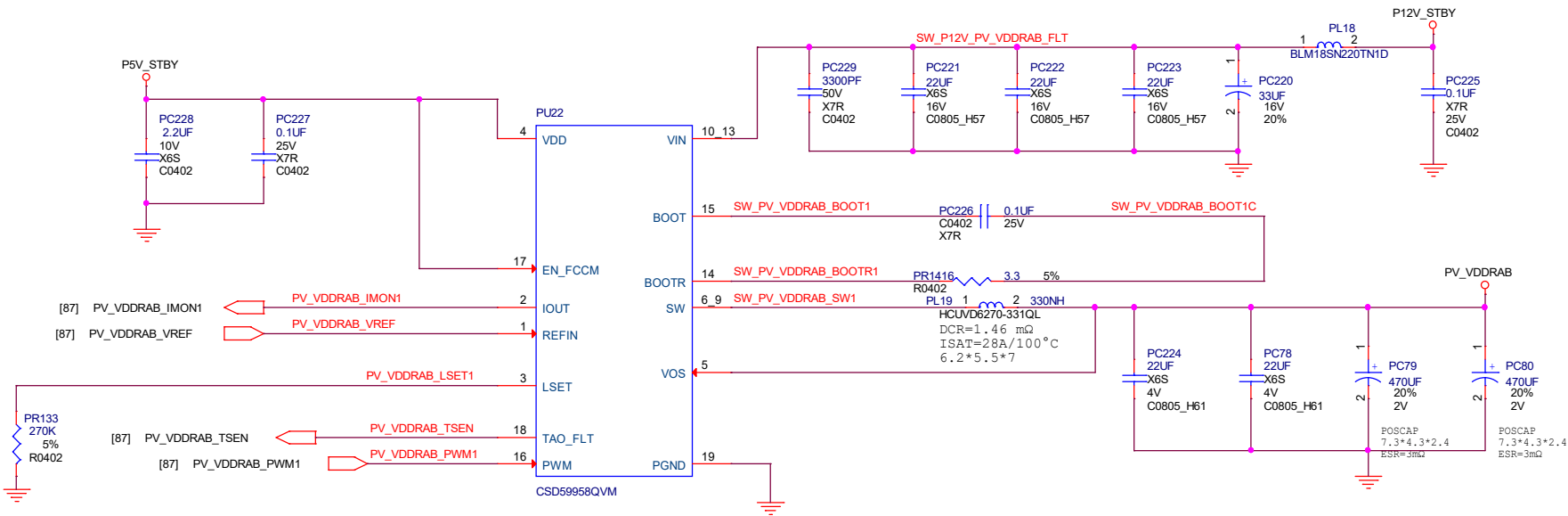
# P1V05\_COMBINED PHASE



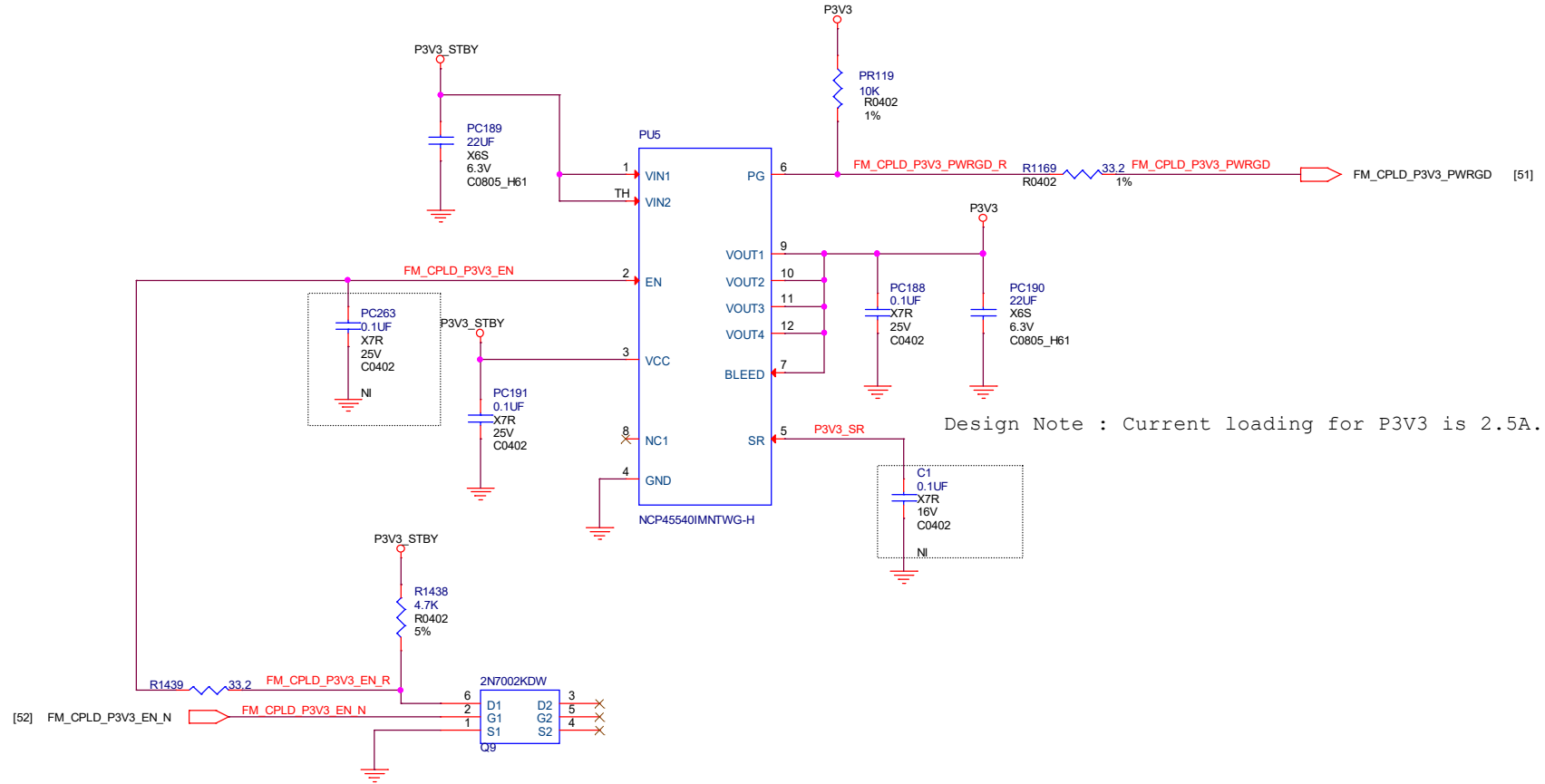


**PV\_VDDRAB Design specification**  
 Output Voltage = 1.215V  
 DC (+/- pk) < 8mV; Vboot=1.2V  
 Ripple (+/- pk) < 2.5mV  
 Total TOL (+/- pk) < 60mV / -40mV (1.26V/1.16V)  
 TDC = 5.93A  
 Max current = 6.27A  
 Over-Current Protection(Max Rating × 1.3) = 8.2A  
 Slew Rate = 16.76A/us  
 Load step = 5.38A  
 Work Frequency = 600kHz  
 Efficiency > 85% @TDC  
 Follow grangeville\_pdg\_2\_2\_p372  
 GVL\_Mem\_Pwr\_Deliv\_TP\_558333\_Rev1\_5

# PV\_VDDRAB\_PHASE1

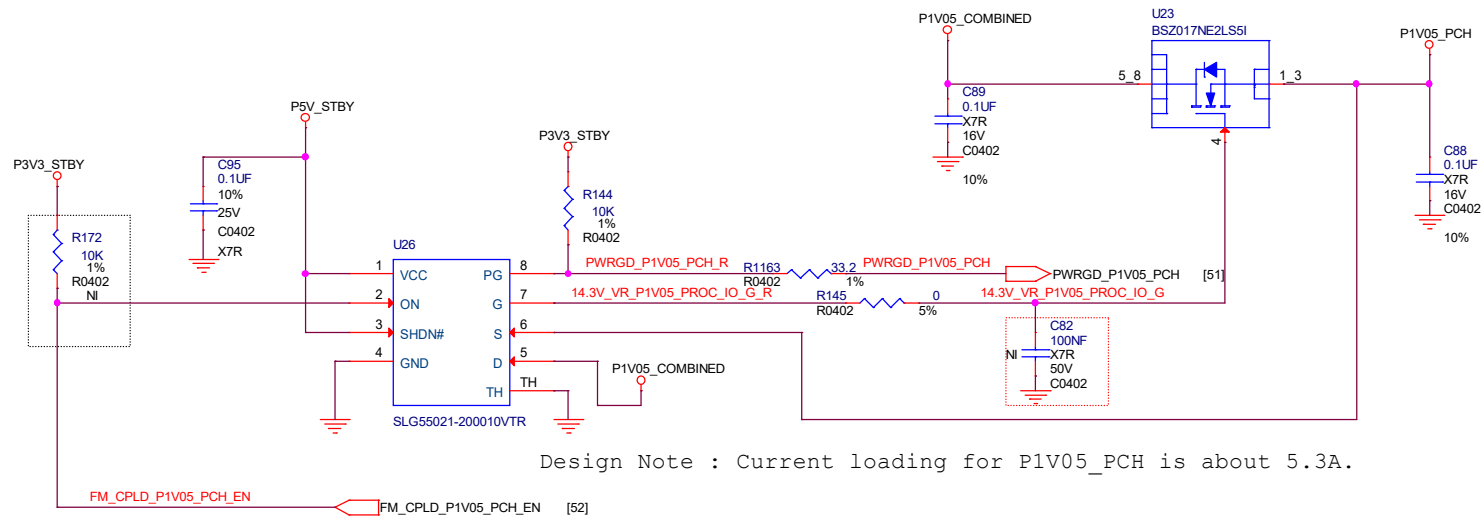






# P3V3 SWITCH

|                                                |            |                                          |           |                        |     |
|------------------------------------------------|------------|------------------------------------------|-----------|------------------------|-----|
| <div> <div>Quanta</div> <div>CCBU</div> </div> | Department | Designer                                 | Project   | Doc Number             | Rev |
|                                                | Reviewer   |                                          | Mini Lake | <Doc>                  | 0.0 |
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# P1V05\_PCH SWITCH



|            |          |           |                                 |                |
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|-------|--|--|--|--|---|--|--|--|--|---|--|--|--|--|---|--|--|--|--|---|--|--|--|--|
| 5     |  |  |  |  | 4 |  |  |  |  | 3 |  |  |  |  | 2 |  |  |  |  | 1 |  |  |  |  |
| D     |  |  |  |  |   |  |  |  |  |   |  |  |  |  |   |  |  |  |  |   |  |  |  |  |
| C     |  |  |  |  |   |  |  |  |  |   |  |  |  |  |   |  |  |  |  |   |  |  |  |  |
| B     |  |  |  |  |   |  |  |  |  |   |  |  |  |  |   |  |  |  |  |   |  |  |  |  |
| A     |  |  |  |  |   |  |  |  |  |   |  |  |  |  |   |  |  |  |  |   |  |  |  |  |
| BLANK |  |  |  |  |   |  |  |  |  |   |  |  |  |  |   |  |  |  |  |   |  |  |  |  |
| 5     |  |  |  |  | 4 |  |  |  |  | 3 |  |  |  |  | 2 |  |  |  |  | 1 |  |  |  |  |

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Department  
CCBU

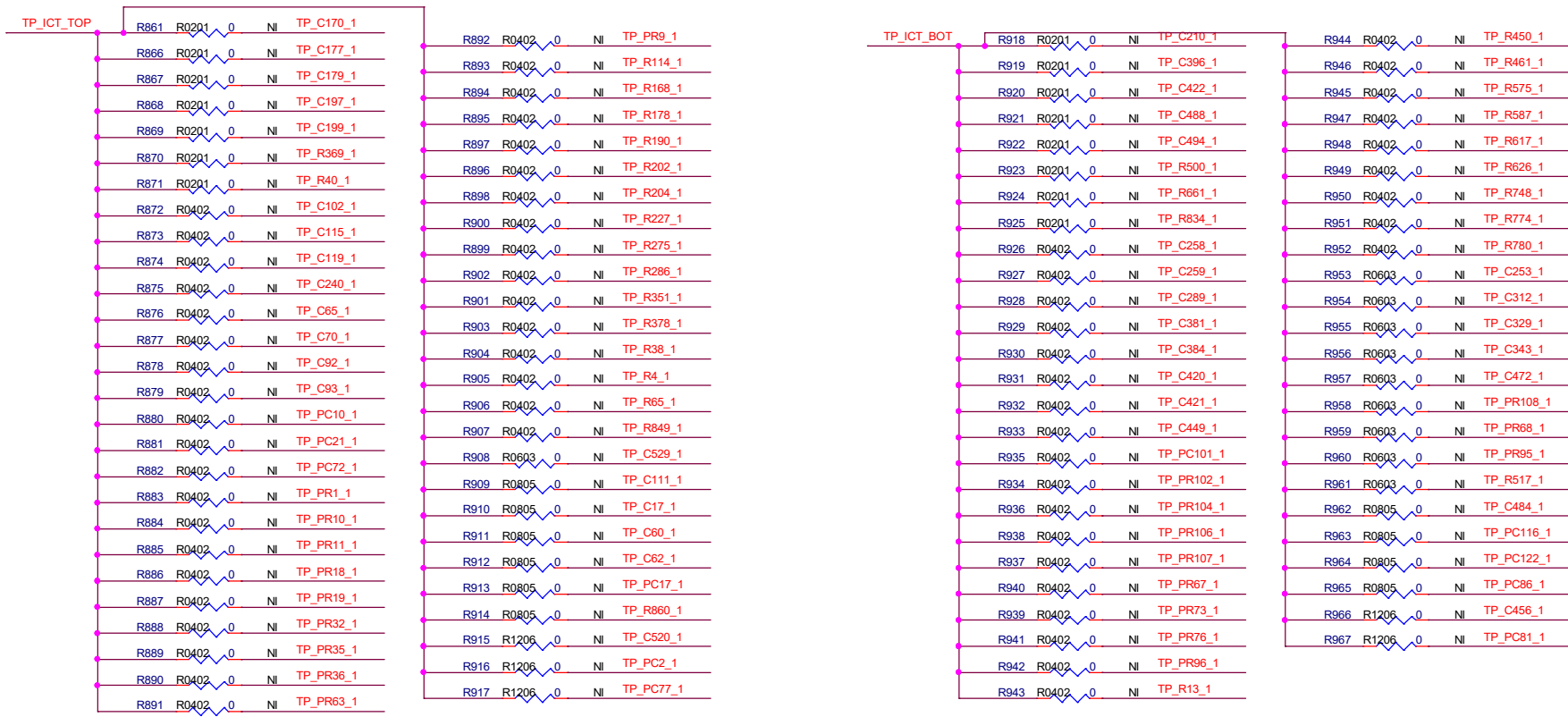
Designer  
Reviewer

Project  
Mini Lake

Doc Number <Doc>  
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# TP RESERVE FOR ICT

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| Reviewer   | Page Title BLANK |                                 |            |                |
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